MASTER OF TECHNOLOGY
In
VLSI & EMBEDDED SYSTEMS

ACADEMIC REGULATIONS, COURSE COVERAGE SUMMARY
&
QUESTION BANK

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
(An Autonomous Institution – UGC, Govt. of India)

Sponsored by CMR Educational Society(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2008 Certified)
Maisammaguda, Dhulapally (Post Via Hakimpet), Secunderabad – 500100, Telangana State, India.
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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

M.TECH – VLSI & EMBEDDED SYSTEMS

R17-COURSE STRUCTURE

I Year I Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R17D6801	VLSI Technology & Design	3	-	3	30	70
2	R17D6802	CPLD & FPGA Architectures& Applications	3	-	3	30	70
3	R17D6803	Embedded System design	3	-	3	30	70
4	R17D6804 R17D6805 R17D6806	ELECTIVE-I 1.Digital System Design 2.CMOS Analog Integrated Circuit Design 3.Hardware Software Co-design	3	-	3	30	70
5	R17D6807 R17D6808 R17D6809	ELECTIVE-II 1.CMOS Digital Integrated Circuit design 2.Algorithms for VLSI Design Automation 3.Advanced Digital Signal Processing	3	-	3	30	70
6	R17DEC51 R17DCS51 R17DME51 R17DAE51	OPEN ELECTIVE –I 1.Embedded Systems Programming 2.Scripting Languages 3.Non-conventional Energy Sources 4.Mathematical Modeling Techniques	3	-	3	30	70
7	R17D6881	VLSI Laboratory	-	3	2	30	70
8	R17D6882	Technical Seminar-I	-	-	2	50	-
Total			18	3	22	260	490

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

I Year II Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R17D6810	Embedded Real Time Operating Systems	3	-	3	30	70
2	R17D6811	CMOS Mixed Signal Circuit Design	3	-	3	30	70
3	R17D6812	Low Power VLSI Design	3	-	3	30	70
4	R17D6813 R17D6814 R17D6815	ELECTIVE – III 1.Adhoc –Wireless Networks 2.Digital Signal Processors & Architectures 3.Embedded Networking	3	-	3	30	70
5	R17D6816 R17D6817 R17D6818	ELECTIVE- IV 1.System On Chip Architecture 2.Design For Testability 3.Multimedia Signal Coding	3	-	3	30	70
6	R17DEC52 R17DCS52 R17DME52 R17DCS53	OPEN ELECTIVE- II 1.Internet of Things 2.Information Security 3.Industrial Management 4.Research Methodology	3	-	3	30	70
7	R17D6883	Embedded Systems Laboratory	-	3	2	30	70
8	R17D6884	Technical Seminar-II	-	-	2	50	-
Total			18	3	22	260	490

II Year I Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R17D6885	Technical Seminar-III	-	-	2	50	-
2	R17D6891	Project Review-I	-	-	10	100	-
3	R17D6892	Project Review-II	-	-	10	100	-
Total			-	-	22	-	-

II Year II Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R17D6886	Technical Seminar-IV	-	-	2	50	-
	R17D6893	Project Review-III	-	-	10	100	-
2	R17D6894	Project Viva-voce	-	-	10	-	100
Total			-	-	22	-	-

I Year I Semester

(R17D6801) VLSI TECHNOLOGY AND DESIGN

UNIT –I:

Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology.Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: I_{ds} –V_{ds} relationships, ThresholdVoltage V T , G m , G ds and ω o , Pass ransistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu} /Z_{pd} , MOSTransistor circuit model, Latch-up in CMOS circuits.

UNIT –II:

Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive andInductive interconnect delays.

UNIT –III:

Combinational Logic Networks:

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks,Gate and Network testing.

UNIT –IV:

Sequential Systems:

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation andtesting.

UNIT –V:

Floor Planning:

Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. EshraghianEshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3 rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2 nd Ed., Addison Wesley.

(R17D6802) CPLD AND FPGA ARCHITECURES AND APPLICATIONS

UNIT-I:

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation

UNIT-II:

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV:

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

(R17D6803) EMBEDDED SYSTEM DESIGN

UNIT –I:

ARM Architecture:

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:

ARM Programming Model – I:

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:

ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:

ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:

Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.
2. Professional Embedded ARM development-James A Langbridge, Wiley/Wrox

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.
2. ARM System on Chip Architecture, Steve Furber, 2nd Edition, Pearson

(R17D6804) DIGITAL SYSTEM DESIGN
(ELECTIVE -I)

UNIT -I:

Minimization and Transformation of Sequential Machines:

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine Minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II:

Digital Design:

Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III:

SM Charts:

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:

Fault Modeling & Test Pattern Generation:

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault Dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques,Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:

Fault Diagnosis in Sequential Circuits:

Circuit Test Approach, Transition Check Approach – State identification and fault detection Experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5 th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2 nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4 th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

(R17D6805) CMOS ANALOG INTEGRATED CIRCUIT DESIGN
(ELECTIVE -I)

UNIT -I:

MOS Devices and Modeling:

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOSDevice Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model forthe MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Currentmirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III:

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High GainAmplifiers Architectures.

UNIT -IV:

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAmp.

UNIT -V:

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-LoopComparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li

(R17D6806) HARDWARE - SOFTWARE CO-DESIGN
(ELECTIVE -I)

UNIT –I:

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent Computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level Specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos System.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.

2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 –Springer

(R17D6807) CMOS DIGITAL INTEGRATED CIRCUIT DESIGN
(ELECTIVE – II)

UNIT –I:

MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage,Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates,Transistor equivalency, CMOS Inverter logic.

UNIT –II:

Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, ComplexLogic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI andOIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:

Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edgetriggered flipflop.

UNIT –IV:

Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOStransmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:

Semiconductor Memories:

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell andrefresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash andNAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3 rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2 nd Ed., PHI.

(R17D6808) ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE-II)

UNIT I

PRELIMINARIES

Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION

Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming,Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING

Problems, Concepts and Algorithms.

MODELLING AND SIMULATION

Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT III

LOGIC SYNTHESIS AND VERIFICATION

Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

HIGH-LEVEL SYNTHESIS

Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aqspects of Assignment problem, High-level Transformations.

UNIT IV

PHYSICAL DESIGN AUTOMATION OF FPGA'S

FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT V

PHYSICAL DESIGN AUTOMATION OF MCM'S

MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley& Sons(Asia) Pvt. Ltd.

2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rdEd., 2005, Springer International Edition.

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.

2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia

(R17D6809) ADVANCED DIGITAL SIGNAL PROCESSING
(ELECTIVE-II)

UNIT I

Review of DFT, FFT, IIR Filters, FIR Filters,

Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of
Multirate Signal Processing

UNIT II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey
Methods, Comparison of all Non-Parametric methods

UNIT III

Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker& Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT –IV

Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm, Properties of Linear Prediction Filters

UNIT V

Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems – Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis& D.G.Manolokis, 4th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
3. DSP – A Pratical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

REFERENCES:

1. Modern spectral Estimation: Theory & Application – S. M .Kay, 1988, PHI.
2. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education

(R17DEC51) EMBEDDED SYSTEMS PROGRAMMING
(OPEN ELECTIVE –I)

Unit 1 - Embedded OS (Linux) Internals

Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication - Semaphore, Pipes, FIFO, Shared Memory
Kernel: Structure, Kernel Module Programming Schedulers and types of scheduling.
Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network

Unit 2 – Open source RTOS

Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, Inter-process communication, Performance Matric in scheduling models, Interrupt management in RTOS environment, Memory management, File systems, I/O Systems, Advantage and disadvantage of RTOS.

Unit 3 – Open Source RTOS Issues

POSIX standards, RTOS Issues - Selecting a Real Time Operating System, RTOS comparative study. Converting a normal Linux kernel to real time kernel, Xenomai basics. Overview of Open source RTOS for Embedded systems (Free RTOS/ Chibios-RT) and application development.

Unit 4 – VxWorks / Free RTOS

VxWorks/ Free RTOS Scheduling and Task Management - Realtime scheduling, Task Creation, Intertask Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts I/O Systems - General Architecture, Device Driver Studies, Driver Module explanation, Implementation of Device Driver for a peripheral

Unit 5 – Case study

Cross compilers, debugging Techniques, Creation of binaries & porting stages for Embedded Development board (Beagle Bone Black, Rpi or similar), Porting an Embedded OS/ RTOS to a target board ().Testing a real time application on the board

TEXT BOOKS:

1. Essential Linux Device Drivers, VenkateswaranSreekrishnan
2. Writing Linux Device Drivers: A Guide with Exercises, J. Cooperstein
3. Real Time Concepts for Embedded Systems – Qing Li, Elsevier

REFERENCES:

1. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill
2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK
3. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society
4. Real-time Systems – Jane Liu, PH 2000
5. Real-Time Systems Design and Analysis: An Engineer's Handbook: Laplante, Phillip A
6. Structured Development for Real - Time Systems V1: Introduction and Tools: Ward, Paul T & Mellor, Stephen J
7. Structured Development for Real - Time Systems V2: Essential Modeling Techniques: Ward, Paul T & Mellor, Stephen J
8. Structured Development for Real - Time Systems V3: Implementation Modeling Techniques: Ward, Paul T & Mellor, Stephen J
9. Monitoring and Debugging of Distributed Real-Time Systems: TSAI, Jeffrey J P & Yang, J H
10. Embedded Software Primer: Simon, David E.
11. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill

(R17DCS51) SCRIPTING LANGUAGES
(OPEN ELECTIVE – I)

UNIT I

Introduction to PERL and Scripting Scripts and Programs, Origin of Scripting , Scripting Today, Characteristics of Scripting Languages, Web Scripting, and the universe of Scripting Languages. PERL-Names and Values, Variables, Scalar Expressions, Control Structures, arrays, list, hashes, strings, pattern and regular expressions, subroutines, advance perl - finer points of looping, pack and unpack, filesystem, eval, data structures, packages, modules, objects, interfacing to the operating system, Creating Internet ware applications, Dirty Hands Internet Programming, security Issues.

UNIT II

PHP Basics- Features, Embedding PHP Code in your Web pages, Outputting the data to the browser, Datatypes, Variables, Constants, expressions, string interpolation, control structures, Function, Creating a Function, Function Libraries, Arrays, strings and Regular Expressions.

UNIT III

Advanced PHP Programming Php and Web Forms, Files, PHP Authentication and Methodologies -Hard Coded, File Based, Database Based, IP Based, Login Administration, Uploading Files with PHP, Sending Email using PHP, PHP Encryption Functions, the Mcrypt package, Building Web sites for the World – Translating Websites- Updating Web sites Scripts, Creating the Localization Repository, Translating Files, text, Generate Binary Files, Set the desired language within your scripts, Localizing Dates, Numbers and Times.

UNIT IV

TCL Structure, syntax, Variables and Data in TCL, Control Flow, Data Structures, input/output, procedures, strings, patterns, files, Advance TCL- eval, source, exec and up level commands, Name spaces, trapping errors, event driven programs, making applications internet aware, Nuts and Bolts Internet Programming, Security Issues, C Interface. Tk- Visual Tool Kits, Fundamental Concepts of Tk, Tk by example, Events and Binding , Perl-Tk.

UNIT V

Python Introduction to Python language, python-syntax, statements, functions, Built-in-functions and Methods, Modules in python, Exception Handling, Integrated Web Applications in Python – Building Small, Efficient Python Web Systems, Web Application Framework.

TEXT BOOKS:

1. The World of Scripting Languages, David Barron, Wiley Publications.
2. Python Web Programming, Steve Holden and David Beazley, New Riders Publications.
3. Beginning PHP and MySQL, 3rd Edition, Jason Gilmore, Apress Publications (Dreamtech)

REFERENCE BOOKS:

1. Open Source Web Development with LAMP using Linux, Apache, MySQL, Perl and PHP, J.Lee and B.Ware (Addison Wesley) Pearson Education.
2. Programming Python, M.Lutz, SPD.
3. PHP 6 Fast and Easy Web Development, Julie Meloni and Matt Telles, Cengage Learning Publications.
4. PHP 5.1, I.Bayross and S.Shah, The X Team, SPD.
5. Core Python Programming, Chun, Pearson Education.
6. Guide to Programming with Python, M.Dawson, Cengage Learning.
7. Perl by Example, E.Quigley, Pearson Education.
8. Programming Perl, Larry Wall, T.Christiansen and J.Orwant, O'Reilly, SPD.
9. Tcl and the Tk Tool kit, Ousterhout, Pearson Education.
10. PHP and MySQL by Example, E.Quigley, Prentice Hall (Pearson).
11. Perl Power, J.P.Flynt, Cengage Learning.
12. PHP Programming solutions, V.Vaswani, TMH.

(R17DME51) NON-CONVENTIONAL ENERGY SOURCES
(OPEN ELECTIVE-I)

UNIT-I

Introduction: Energy Scenario, Survey of energy resources. Classification and need for conventional energy resources.

Solar Energy: The Sun-sun-Earth relationship, Basic matter to waste heat energy circuit, SolarRadiation, Attention, Radiation measuring instruments.

Solar Energy Applications: Solar water heating. Space heating, Active and passive heating, Energystorage, Selective surface, Solar stills and ponds, solar refrigeration, Photovoltaic generation.

UNIT -II

Geothermal Energy: Structure of earth, Geothermal Regions, Hot springs. Hot Rocks, HotAquifers. Analytical methods to estimate thermal potential. Harnessing techniques, Electricity generating systems.

UNIT-III

Direct Energy Conversion: Nuclear Fusion, Fusion reaction, P-P cycle, Carbon cycle, Deuterium cycle, Condition for controlled fusion, Fuel cells and photovoltaic, Thermionic and Thermoelectric generation and MHD generator.

Hydrogen Gas as Fuel: Production methods, Properties, I.C. Engines applications, Utilization strategy, Performances.

UNIT-IV

Bioenergy: Biomass energy sources. Plant productivity, Biomass wastes, aerobic and anaerobicbioconversion processes, Raw material and properties of bio-gas, Bio-gas plant technology and status, the energetic and economics of biomass systems, Biomass gasification

UNIT-V

Wind Energy: Wind, Beaufort number, Characteristics, Wind energy conversion systems, Types, Betz model. Interference factor. Power coefficient, Torque coefficient and Thrust coefficient, Lift machines and Drag machines. Matching Electricity generation.

Energy from Oceans: Tidal energy, Tides, Diurnal and semi-diurnal nature, Power from tides, WaveEnergy, Waves, Theoretical energy available. Calculation of period and phase velocity of waves, Wave power systems, submerged devices. Ocean thermal Energy, Principles, Heat exchangers, Pumping requirements, Practical considerations.

TEXTBOOKS:

1. Non-conventional Energy Sources / GD Rai/Khanna publications.
2. Non-Conventional Energy Sources and Utilisation (Energy Engineering)/ R KRajput/ S.Chand.
3. Renewable Energy Sources /Twidell& Weir/Taylor and Francis/ 2nd special Indian edition.

REFERENCE BOOKS:

1. Renewable Energy Resources- Basic Principles and Applications/ G.N.Tiwari and M.K.GhosalNarosa Publications.
2. Renewable Energy Resources/ John Twidell& Tony Weir/Taylor & Francis/2nd edition.
3. Non Conventional Energy / K.Mittal/ Wheeler.

(R17DAE51) MATHEMATICAL MODELING TECHNIQUES
(OPEN ELECTIVE-I)

UNIT-I: **INTRODUCTION TO MODELING AND SINGULAR PERTURBATION METHODS**

Definition of a model, Procedure of modeling: problem identification, model formulation, reduction, analysis, Computation, model validation, Choosing the model, Singular Perturbations: Elementary boundary layer theory, Matched asymptotic expansions, Inner layers, nonlinear oscillations

UNIT-II: **VARIATIONAL PRINCIPLES AND RANDOM SYSTEMS**

Variational calculus: Euler's equation, Integrals and missing variables, Constraints and Lagrange multipliers, Variational problems: Optics-Fermat's principle, Analytical mechanics: Hamilton's principle, Symmetry: Noether's theorem, Rigid body motion, Random systems: Random variables, Stochastic processes, Monte Carlo method

UNIT-III: **FINITE DIFFERENCES: ORDINARY AND PARTIAL DIFFERENTIAL EQUATIONS**

ODE: Numerical approximations, Runge-Kutta methods, Beyond Runge-Kutta, PDE: Hyperbolic equations-waves, Parabolic equations-diffusion, Elliptic equations-boundary values

CELLULAR AUTOMATA AND LATTICE GASES

Lattice gases and fluids, Cellular automata and computing

UNIT- IV: **FUNCTION FITTING AND TRANSFORMS**

Function fitting: Model estimation, Least squares, Linear least squares: Singular value decomposition, Non-linear least squares: Levenberg-Marquardt method, Estimation, Fisher information, and Cramer-Rao inequality, Transforms: Orthogonal transforms, Fourier transforms, Wavelets, Principal components

FUNCTION FITTING ARCHITECTURES

Polynomials: Pade approximants, Splines, Orthogonal functions, Radial basis functions, Over-fitting, Neural networks: Back propagation, Regularization

UNIT-V: **OPTIMIZATION AND SEARCH**

Multidimensional search, Local minima, Simulated annealing, Genetic algorithms

FILTERING AND STATE ESTIMATION

Matched filters, Wiener filters, Kalman filters, Non-linearity and entrainment, Hidden Markov models

TEXT BOOKS

1. *The Nature of Mathematical Modeling*, Neil Gershenfeld, Cambridge University Press, 2006,ISBN 0-521-57095-6

REFERENCE BOOKS

1. *Mathematical Models in the Applied Sciences*, A. C. Fowler, Cambridge University Press, 1997,ISBN 0-521-46140-5
2. *A First Course in Mathematical Modeling*, F. R. Giordano, M.D. Weir and W.P. Fox, 2003,Thomson, Brooks/Cole Publishers
3. *Applied Numerical Modeling for Engineers*, Donald De Cogan, Anne De Cogan, Oxford UniversityPress, 1997

(R17D6881) VLSI LABORATORY

Note:
Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design,Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulationand verification.

Part –I: VLSI Front End Design programs:
Programming can be done using any complier. Down load the programs on FPGA/CPLD boards andperformance testing may be done using pattern generator (32 channels) and logic analyzer apart fromverification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, CarryLook Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequencecounter
11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, multiplication and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits

Part –II: VLSI Back End Design programs:

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area,performance and/or power, Layout, Extraction of parasitic and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1.Introduction to layout design rules
2.Layout, physical verification, placement & route for complex design, static timing Analysis, IR drops analysis and crosstalk analysis of the following:

- Basic logic gates
- CMOS inverter
- CMOS NOR/ NAND gates
- CMOS XOR and MUX gates
- CMOS 1-bit full adder
- Static / Dynamic logic circuit (register cell)
- Latch
- Pass transistorBasic logic gates

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths

I Year II Semester

(R17D6810) EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT – I:
Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read,write), Process Control (fork, vfork, exit, wait, waitpid, exec.

UNIT - II:
Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS,Defining a Task asks States and Scheduling, Task Operations, Structure, Synchronization,
Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:
Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:
Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V:
Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:
1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011
REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

(R17D6811) CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT -I:

Switched Capacitor Circuits:

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing,biquad filters.

UNIT -II:

Phased Lock Loop (PLL):

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities,Jitter in PLLs, Delay locked loops, applications

UNIT -III:

Data Converter Fundamentals:

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:

Nyquist Rate A/D Converters:

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V:

Oversampling Converters:

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press,International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche,Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

(R17D6812) LOW POWER VLSI DESIGN

UNIT –I:

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation,Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, ShortChannel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, VelocitySaturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques– Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons,2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

(R17D6813) ADHOC –WIRELESS NETWORKS
(ELECTIVE -III)

UNIT -I:

Wireless LANS and PANS: Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.
AD HOC Wireless Networks: Introduction, Issues in Ad Hoc Wireless Networks.

UNIT -II:
MAC Protocols: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT -III:
Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT –IV:
Transport Layer Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT –V:
Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS:
1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.
REFERENCE BOOKS:
1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh , 1st Ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer.

(R17D6814) DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(ELECTIVE -III)

UNIT –I:

Introduction to Digital Signal Processing:
Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences.Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems,Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:

Architectures for Programmable DSP Devices:
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:

Programmable Digital Signal Processors:
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:

Analog Devices Family of DSP Devices:
Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.
Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture,Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices:
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture
Publisher: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by the Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D.,California Technical Publishing, ISBN 0-9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes ISBN 0750679123, 2005

(R17D6815) EMBEDDED NETWORKING
(ELECTIVE -III)

UNIT –I:

Embedded Communication Protocols:

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire

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UNIT –II:

USB and CAN Bus:

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication:Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III:

Ethernet Basics:

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV:

Embedded Ethernet:

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V:

Wireless Embedded Networking:

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari?, Cambridge press 2005.

(R17D6816) SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -IV)

UNIT –I:

Introduction to the System Approach:

System Architecture, Components of the system, Hardware & Software, Processor

UNIT –II:

Processors:

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.Simple Processor – memory interaction.

UNIT –III:

Memory Design for SOC:

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT -IV:

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:

Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG Compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2 nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1 st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

(R17D6817) DESIGN FOR TESTABILITY
(ELECTIVE -IV)

UNIT -I:
Introduction to Testing:
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:
Logic and Fault Simulation:
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III:
Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and **Scan Design:** Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:
Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation,N Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:
Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pi n Descriptions.

TEXT BOOKS:
1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:
1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Frieman, Jaico Publishing House
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press..

(R17D6818) MULTIMEDIA AND SIGNAL CODING
(ELECTIVE-IV)

UNIT-I: Introduction to Multimedia: Multimedia, World Wide Web, and Overview of Multimedia Tools, Multimedia Authoring, Graphics / Image Data Types, and File Formats.

Color in Image and Video: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Out-of-Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

UNIT-II: Video Concepts: Types of Video Signals, Analog Video, Digital Video.

Audio Concepts: Digitization of Sound, Quantization and Transmission of Audio.

UNIT-III: Compression Algorithms:

Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.

Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet Based Coding.

Image Compression Standards: JPEG and JPEG2000.

UNIT-IV:

Video Compression Techniques: Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and InterFrame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT-V:

Audio, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

TEXT BOOKS:

1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.
2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition, 2009.

REFERENCE BOOKS:

1. Multimedia Communication Systems – Techniques, Stds & Netwroks K.R. Rao, Zorans. Bojkoric, Dragorad A. Milovanovic, 1st Edition, 2002.
2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition, 2009.
3. Multimedia Systems John F. Koegel Bufond Pearson Education (LPE), 1st Edition, 2003.
4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.

Video Processing and Communications – Yaowang, Jorn Ostermann, Ya-QinZhang, Pearson, 2002

(R17DEC52) INTERNET OF THINGS
(OPEN ELECTIVE –II)

Unit 1: The IoT Networking Core:

Technologies involved in IoT Development: Internet/Web and Networking Basics OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing IoT Platform overview Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

Unit 2: Network Fundamentals:
Overview and working principle of Wired Networking equipment's – Router, Switches, Overview and working principle of Wireless Networking equipment's – Access Points, Hubs etc. Linux Network configuration Concepts: Networking configurations in Linux Accessing Hardware & Device Files interactions.

Unit 3: IoT Architecture:
History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols Applications: Remote Monitoring & Sensing, Remote Controlling, and Performance Analysis. The Architecture the Layering concepts, IoT Communication Pattern, IoT protocol Architecture, The 6LoWPAN Security aspects in IoT

Unit 4: IoT Application Development:
Application Protocols MQTT, REST/HTTP, CoAP, MySQL.
Back-end Application Designing
Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS & jQuery for UI Designing, JSON lib for data processing, Security & Privacy during development, Application Development for mobile Platforms: Overview of Android / IOS App Development tools

Unit 5: Case Study & advanced IoT Applications:
IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)

TEXT BOOKS:
1. 6LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. Ovidiu Vermesan, Dr. Peter Friess, River Publishers
3. Interconnecting Smart Objects with IP: The Next Internet, Jean-Philippe Vasseur, Adam Dunkels, Morgan Kuffmann

REFERENCES:

1. The Internet of Things: From RFID to the Next-Generation Pervasive Networked Lu Yan, Yan Zhang, Laurence T. Yang, Huansheng Ning
2. Internet of Things (A Hands-on-Approach), Vijay Madisetti , Arshdeep Bahga
3. Designing the Internet of Things, Adrian McEwen (Author), Hakim Cassimally
4. Asoke K Talukder and Roopa R Yavagal, "Mobile Computing," Tata McGraw Hill, 2010.
5. Computer Networks; By: Tanenbaum, Andrew S; Pearson Education Pte. Ltd., Delhi, 4th Edition
6. Data and Computer Communications; By: Stallings, William; Pearson Education Pte. Ltd., Delhi, 6th Edition
7. F. Adelstein and S.K.S. Gupta, "Fundamentals of Mobile and Pervasive Computing," McGraw Hill, 2009.
8. Cloud Computing Bible, Barrie Sosinsky, Wiley-India, 2010.
9. Cloud Security: A Comprehensive Guide to Secure Cloud Computing, Ronald L. Krutz, Russell Dean Vines, Wiley-India, 2010

(R17DCS52) INFORMATION SECURITY
(OPEN ELECTIVE – II)

UNIT I

A model for Internetwork security, Conventional Encryption Principles & Algorithms (DES, AES, RC4, Blowfish), Block Cipher Modes of Operation, Location of Encryption Devices, Key Distribution. Public key cryptography principles, public key cryptography algorithms (RSA, Diffie-Hellman, ECC), public Key Distribution.

UNIT II

Approaches of Message Authentication, Secure Hash Functions (SHA-512, MD5) and HMAC, Digital Signatures, Kerberos, X.509 Directory Authentication Service, Email Security: Pretty Good Privacy (PGP)
IP Security: Overview, IP Security Architecture, Authentication Header, Encapsulating Security Payload, Combining Security Associations and Key Management.

UNIT III

Web Security: Requirements, Secure Socket Layer (SSL) and Transport Layer Security (TLS), Secure Electronic Transaction (SET). Firewalls: Firewall Design principles, Trusted Systems, Intrusion Detection Systems

UNIT IV

Auditing For Security: Introduction, Basic Terms Related to Audits, Security audits, The Need for Security Audits in Organization, Organizational Roles and Responsibilities for Security Audit, Auditors Responsibility In Security Audits, Types Of Security Audits.

UNIT V

Auditing For Security: Approaches to Audits, Technology Based Audits Vulnerability Scanning And Penetration Testing, Resistance to Security Audits, Phase in security audit, Security audit Engagement Costs and other aspects, Budgeting for security audits, Selecting external Security Consultants, Key Success factors for security audits.

TEXT BOOKS:

1. Cryptography and Network Security by William Stallings, Fourth Edition, Pearson Education 2007.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education, 2008.
3. Cryptography & Network Security by Behrouz A. Forouzan, TMH 2007.
4. Information Systems Security by Nina Godbole, WILEY 2008.

REFERENCE BOOKS:

1. Information Security by Mark Stamp, Wiley – INDIA, 2006.
2. Fundamentals of Computer Security, Springer.
3. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH
4. Computer Security Basics by Rick Lehtinen, Deborah Russell & G.T.Gangemi Sr., SPD O'REILLY 2006.
5. Modern Cryptography by Wenbo Mao, Pearson Education 2007.
6. Principles of Information Security, Whitman, Thomson.

(R17DME52) INDUSTRIAL MANAGEMENT
(OPEN ELECTIVE-II)

UNIT- I

Concepts of Management and Organisation - Functions of Management - Evolution of Management Thought : Taylor's Scientific Management, Fayol's Principles of Management, Douglas Mc-Gregor's Theory X and Theory Y, Mayo's Hawthorne Experiments, Hertzberg's Two Factor Theory of Motivation, Maslow's Hierarchy of Human Needs - Systems Approach to Management.

UNIT –II

Designing Organisational Structures : Basic concepts related to Organisation - Departmentation and Decentralisation, Types of mechanistic and organic structures of organisation (Line organization, Line and staff organization, functional organization, Committee organization, matrix organization, Virtual Organisation, Cellular Organisation, team structure, boundaryless organization, inverted pyramid structure, lean and flat organization structure) and their merits, demerits and suitability.

UNIT –III

Plant location, definition, factors affecting the plant location, comparison of rural and urban sites-methods for selection of plant- Matrix approach. Plant Layout - definition, objectives, types of production, types of plant layout - various data analyzing forms-travel chart. Work study - Definition, objectives, method study - definition, objectives, steps involved- various types of associated charts-difference between micromotion and memomotion studies. Work measurement-definition, time study, steps involved-equipment, different methods of performance rating- allowances, standard time calculation. Work Sampling - definition, steps involved, standard time calculations, and differences with time study.

UNIT –IV

Materials Management-Objectives, Inventory - functions, types, associated costs, inventory classification techniques-ABC and VED analysis. Inventory Control Systems-Continuous review system-periodical review system. Stores Management and Stores Records. Purchase management, duties of purchase of manager,associated forms.Introduction to PERT / CPM : Project management, network modeling-probabilistic model, various types of activity times estimation-programme evaluation review techniques-Critical Path-probability of completing the project, deterministic model, critical path method (CPM)-critical path calculation-crashing of simple of networks.

UNIT –V

Inspection and quality control, types of inspections - Statistical Quality Control-techniques-variables and attributes-assignable and non assignable causes- variable control charts, and R charts, attributes control charts, p charts and c charts. Acceptance sampling plan- single sampling and double sampling plans-OC curves. Introduction to TQM-Quality Circles, ISO 9000 series procedures. Introduction to Human Resource Management, Functions of HRM, Job Evaluation, different types of evaluation methods. Job description, Merit Rating.- difference with job evaluation, different methods of merit ratings, wage incentives, different types of wage incentive schemes. Marketing, marketing vs selling, marketing mix, productlife-cycle.

TEXT BOOKS:

1. Amrine, Manufacturing Organization and Management, Pearson, 2nd Edition, 2004.
2. Industrial Engineering and Management O.P. Khanna Dhanpat Rai.
3. A.R.Aryasri, Management Science , Tata McGraw-Hill, 2002.

REFERENCE BOOKS:

1. Panner Selvam, Production and Operations Management, PHI, 2004.
2. Dr. C. Nadha Muni Reddy and Dr. K. Vijaya Kumar Reddy, Reliability Engineering & Quality Engineering, Galgotia Publications, Pvt., Limited.
3. Phillip Kotler, Marketing Management, Pearson, 2004.

(R17DCS53) RESEARCH METHODOLOGY
(OPEN ELECTIVE – II)

UNIT - I

Introduction: Research objective and motivation, Types of research, Research approaches, Significance, Research method vs. methodology, Research process.

UNIT - II

Formulating a research problem: Literature review, Formulation of objectives, Establishing Operational definitions, Identifying variables, constructing hypotheses.

UNIT - III

Research design and Data Collection: Need and Characteristics, Types of research design, Principles of Experimental research design, Method of data collection, Ethical issues in collecting data.

UNIT - IV

Sampling and Analysis of data: Need of Sampling, Sampling distributions, Central limit theorem, Estimation: mean and variance, Selection of sample size Statistics in research, Measures of Central tendency, Dispersion, asymmetry and relationships, Correlation and Regression analysis, Displaying data

UNIT - V

Hypothesis Testing: Procedure, Hypothesis testing for difference in mean, variance limitations, Chi-square test, Analysis of variance (ANOVA), Basic principles and techniques of writing a Research Proposal

Text Books:

1. R. C. Kothari, Research Methodology: Methods and Techniques, 2nd edition, New Age International Publisher, 2009

2. Ranjit Kumar, Research Methodology: A Step-by-Step Guide for Beginners, 2nd Edition, SAGE, 2005

References:

1. Trochim, William M. The Research Methods Knowledge Base, 2nd Edition. Internet WWW page, at URL: <http://www.socialresearchmethods.net/kb/>

2. (Electronic Version): StatSoft, Inc. (2012). Electronic Statistics Textbook. Tulsa, OK: StatSoft. WEB: http://www.statsoft.com/textbook/.(Printed Version): Hill, T. & Lewicki, P. (2007). STATISTICS: Methods and Applications. StatSoft, Tulsa, OK.

(R17D6883) EMBEDDED SYSTEMS LABORATORY

Note:
The following programs are to be implemented on ARM based Processors/Equivalent.
Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

Part -I: The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for a. Addition | Subtraction | Multiplication | Division
b. Operating Modes, System Calls and Interrupts
c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

Part -II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs (Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

I YEAR I SEMESTER

COURSE COVERAGE SUMMARY & QUESTION BANK

VLSI TECHNOLOGY AND DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	CHAPTERS IN TEXT BOOK	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Essentials of VLSI Circuits and Systems	1,2	UNIT-I:Review of Microelectronics and Introduction to MOS Technologies	K. Eshraghian Eshraghian. D, A. Pucknell	PHI	2005
2	Modern VLSI Design	2,3	UNIT –II: Layout Design and Tools	Wayne Wolf	Pearson Education	3 rd Ed
3	Modern VLSI Design	4	UNIT –II: Combinational Logic Networks	Wayne Wolf	Pearson Education	3 rd Ed
4	Modern VLSI Design	5	UNIT –IV: Sequential Systems	Wayne Wolf	Pearson Education	3 rd Ed
5	Modern VLSI Design	7,8	UNIT –V: Floor Planning	Wayne Wolf	Pearson Education	3 rd Ed

Code No: R15D6801

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Aug 2017
VLSI Technology & Design
(VLSI & ES)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing one Question from each section and each Question carries 15 marks.

SECTION – I

1. (a) What is pass transistor and explain its circuit and characteristics
   (b) What is the operating principle of inverter. Explain CMOS inverter with circuit diagram (8+7)

(Or)

2. (a) Explain the significance of GATE DRAIN and SOURCE terminals in MOSFET with neat sketch
   (b) Explain LATCH-UP in CMOS circuits with example . (7+8)

SECTION – II

3. (a) Explain the principle of operation of static complementary gate with neat sketch.
   (b) Explain resistive delays in interconnections of gates. (8+7)

(Or)

4. (a) Explain the principle of operation of low power gate with neat sketch
   (b) Explain inductive delays in interconnections of gates (7+8)

SECTION – III

5. (a) Explain different types of GATE designs used with advantages and disadvantages.
   (b) Explain different types of logic levels used in GATES (8+7)

(Or)

6. (a) Explain the advantages of simulation and its procedure in VLSI design tools.
   (b) With neat Block Diagram explain different methods of designs in interconnection of gates in single layer layout. (8+7)

SECTION – IV

7. (a) Explain the process of layout with neat sketch.
   (b) Explain different techniques used in estimating propagation delays (8+7)

(Or)

8. (a) Explain the advantages and disadvantages of power optimization techniques
   (b) Explain the need of delay estimation in VLSI design (8+7)

SECTION – V

9. Explain different off-chip connections (15)

(Or)

10. What is global interconnect and explain its advantages and disadvantages (15)

Code No: R15D6801

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech. I Semester Regular/supplementary Examinations, February 2017

VLSI Technology & Design

(VLSI&ES)

Roll No			N	3						

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

* * * * * *

SECTION – I

1. (a) Explain the differences between CMOS, MOS, and BiCMOS technologies.
   (b) Explain the I_{DS}-V_{DS} relationship of CMOS transistor with neat sketch (8+7)

(Or)

2. (a) Explain the significance of threshold voltage with respect to transistor.
   (b) Explain the properties of CMOS, MOS, and BiCMOS technologies. (7+8)

SECTION – II

3. (a) Explain about different types of transistor structures used in layout design.
   (b) What is scalability in layout design and the rules of scalability (8+7)

(Or)

4. (a) Explain different tools used in layout design with advantages and disadvantages.
   (b) Explain multilayer layout designs with advantages and disadvantages (7+8)

SECTION – III

5. (a) Explain different types of layouts used with advantages and disadvantages.
   (b) Explain different types of logic levels used in switches (8+7)

(Or)

6. (a) Explain the need of simulation and its procedure in VLSI design.
   (b) With neat Block Diagram explain different methods of designs in interconnection of gates in multilayer layout. (8+7)

SECTION – IV

7. (a) Explain the need of memory cell and its construction with neat sketch.
   (b) Explain different techniques used in clocking disciplines (8+7)

(Or)

8. (a) Explain different constructional details of memory arrays with neat sketch
   (b) Explain the need of layout in VLSI design (8+7)

SECTION – V

9. Explain different types of floor planning methods . (15)

(Or)

10. Explain different types of designs used in floor planning with neat sketch (15)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6801

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018
VLSI Technology & Design
(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

Section-I

1.a. With a neat diagram, Explain CMOS Inverter voltage transfer characteristics with a neat diagram? 8M
b. Compare CMOS and Bipolar technologies. 7M

Or

2. aDerive the relevant expressions I_{ds} versus V_{ds} in the non saturated and saturated regions.8M
b. Briefly explain about V_t, g_m,g_{ds}, w_o of MOS transistor.7M

Section-II

3.a What are the varieties of design layout of wiring trees in the wires and delay? 8M
b. What are design rules? Why is metal-metal spacing larger then poly-poly spacing preferred? 7M

Or

4.a. What are lambda based design rules? Give them for each layer. 8M
b. Draw the stick diagram of 2-input Ex-or gate. 7M

Section-III

5.a. How the standard cell layout design of a combinational logic network is implemented? Explain. 8M
b. Mention the various approaches of routing techniques to equalize channel utilization. 7M

Or

6.a. What are the problems presented by power distribution? How they are solved? 8M
b. How fan-out and path delay influences delay in combinational networks. Explain. 7M

Section-IV

7. Explain about clocking disciplines 15M

Or

8. Explain the methods for testing faulty gate in a combinational network. 15M

Section-V

9. a. Briefly Explain about floor planning methods. 8M
b. What are various interconnect models and the factors effecting inter connect performance. 7M

Or

10.a. Name the purposes and basic ideas for floor planning? 8M
b. Discuss the design of floor plan and its considerations? 7M

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D6801 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Regular Examinations, Jan/Feb 2018
VLSI Technology& Design
(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

*****

SECTION - I

1.(a) What are the electrical properties of MOS and CMOS. (7m)
(b) Compare CMOS and BiCMOS technologies. (7m)

or

2 (a) Draw the diagram of CMOS & BiCMOS inverters and explain about them. (7m)
(b) List out the limitations of MOS and BiCMOS technologies. (7m)

SECTION - II

3.(a) What is the need of Layout design, Explain about the latest layout design and give its significance. (7m)
(b) List out various Scalable design rules and explain about them. (7m)

or

4 (a) Compare resistive and inductive interconnect delays. (7m)
(b) Explain in detail about Static complementary gates with example. (7m)

SECTION - III

5 Explain in detail about the following with respect to Combinational logic networks. (14m)
i) Layouts
ii) Gate testing

Or

6 Explain in detail about Interconnect design with example with respect to switch logic networks. (14m)

SECTION – IV

7 What is the need of Design validations and testing with respect to sequential systems and explain about them. (14m)

Or

8 What do you understand by the term Clocking disciplines and explain about them in detail. (14m)

SECTION – V

9 Discuss in detail about Global interconnect with regards to Floor Planning. (14m)

Or

10 What is the need of Floor planning methods and explain in detail any two methods (14m)

Code No: R15D6801 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
VLSI Technology & Design
(VLSI&ES)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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Section-I

Q. No. 1 a) Derive the I_{ds} – V_{ds} relationships and figure of merit of a NMOS transistor (10M)
b) Discuss about the Latch-up in CMOS circuits with suitable diagrams. (5M)

OR

Q. No. 2 a) Explain the CMOS fabrication using N-well process with neat diagrams (8M)
b) Compute the Z_{pu} /Z_{pd} when the inverter is driven by one or more pass transistors. (7M)

Section-II

Q. No. 3 a) Discuss about the Scalable design rules in detail with relevant diagrams (10M)
b) Draw the structure of AND-NAND logic using DCVSL (5M)

OR

Q. No. 4 a) Draw the layout diagram of a static complementary gate that computes [a (b+c)]' (10M)
b) Discuss about any one method used in the design of low power gates (5M)

Section-III

Q. No. 5 a) Categorize the types of Simulators and explain the switch level simulation. (5M)
b) How could you determine the fault testing for combinational networks? (5M)
c) What changes would you make to optimize the power consumption ? (5M)

OR

Q. No. 6 a) Can you elaborate how to design logic networks using realistic interconnect models? (8M)
b) Briefly discuss about the Left-edge channel routing and channel density in standard cell layout. (7M)

Section-IV

Q. No. 7 a) Discuss in detail about Clocking disciplines to construct a sequential system (12M)
b) Draw the structure of an LSSD latch. (3M)

OR

Q. No. 8 Explain briefly about design validation and testing. (15M)

Section-V

Q. No. 9 briefly discuss about the Floor Planning Methods. (15M)

OR

Q. No. 10 a) Explain the Floor Plan Design (7M)
b) Briefly discuss about the I/O architecture and Pad design (8M)

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D6801

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
VLSI Technology & Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION - I

1.(a) Differentiate between CMOS and BICMOS technologies. (7M)

(b) Explain in detail about Latch –up in CMOS circuits. (7M)

(OR)

2 (a) Discuss in detail about MOS Transistor circuit model. (7M)

(b) Draw and explain the operation of CMOS inverter and its characteristics. (7M)

SECTION - II

3.(a) List out various Layout design tools and explain about them. (7M)

(b) Explain with example in detail, about Wires and Vias. (7M)

(OR)

4 (a) What are Static complementary gates .Explain about them in detail. (7M)

(b) Compare the Scalable design rules and Layout design. (7M)

SECTION – III

5 Define the term Power Optimization and explain about the term related to combinational logic networks .(14M)

(OR)

6 With respect to combinational logic circuits, explain the following terms
   (i) Network delay (7M)
   (ii) Network testing (7M)

SECTION – IV

7 Explain the concept of Power Optimization for Sequential systems with an example. (14M)

(OR)

8 List out and explain about the Memory cells and Array with respect to the sequential circuits (14M)

SECTION – V

9 What is the need of floor planning methods and explain in details any two methods. (14M)

(OR)

10 What are Off–chip connections? List out the advantages and limitations. (14M)

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CPLD AND FPGA ARCHITECURES AND APPLICATIONS

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	CHAPTERS IN TEXT BOOK	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS
1	Digital Systems Design	2,3	Unit I- Introduction to Programmable Logic Devices	Charles H. Roth Jr, Lizy Kurian John	Cengage Learning
2	Field Programmable Gate Array Technology	2,3	UNIT-II: Field Programmable Gate Arrays	Stephen M. Trimberger,	Springer International Edition
3	Field Programmable Gate Array Technology	4	UNIT -III: SRAM Programmable FPGAs	Stephen M. Trimberger,	Springer International Edition
4	Field Programmable Gate Array Technology	5	UNIT -IV: Anti-Fuse Programmed FPGAs	Stephen M. Trimberger,	Springer International Edition
5	Field Programmable Gate Array Technology	7,8	UNIT -V: Design Applications	Stephen M. Trimberger,	Springer International Edition

Code No: R15D6802 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech. I Semester Regular/supplementary Examinations, February 2017

CPLD & FPGA Architectures & Applications

(VLSI&ES)

Roll No			N	3						

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

* * * * * *

SECTION – I

1.Explain the Applications of CPLD &FPGAs in digital design.

(OR)

2.Distinguish among ROM, PLA, PAL.

SECTION – II

3. Draw and explain programmable interconnects, programmable i/o blocks in FPGAs.

(OR

4. Discuss about the dedicated specialized components of FPGAs and their Applications of FPGAs..

SECTION – III

5. a) What are the salient features of XC2000 FPGA CLB?
   b) What are the salient features of Altera's FLEX 4000 FPGA logic element?

(OR)

6. Discuss the device architecture for XC3000 FPGA logic element and CLB?

SECTION – IV

7. How would you implement the function Y = ABC using Actel Act2 FPGA?

(OR)

8. Explain the device architecture for ACT1 and ACT2.

SECTION – V

9. What are the features of a fast video controller, a position tracker for a robot manipulator?

(OR)

10. How would you implement a binary counter using the CLBs of FPGA?

*****

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D6802 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Regular Examinations, Jan/Feb 2018
CPLD& FPGA Architectures Applications
(VLSI& ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

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Section-I

Q. No. 1 a) Design a XNOR gate with PLA and PAL (7M)
b) Design a XOR gate with PROM and ROM (7M)

OR

Q. No. 2 a) Design a Boolean expression f=AB+BC+CA with PROM (7M)
b) Design a Boolean expression f=ABC+BCD+CA with PLA (7M)

Section-II

Q. No. 3 a) Explain FPGA state machine terms: i) State transition table, ii) State table. (7M)

b) What are the basic concepts and properties of Petrinet and explain it. (7M)

OR

Q. No. 4 a) Explain the design flow of CPLD and FPGA. (7M)

b) Mention various digital front end digital design tools for FPGA & ASICs. (7M)

Section-III

Q. No. 5 a) Draw and explain the architecture of Cypress Flash 370 CPLD. (7M)
b) Mention the features of a Lattice isp & PLSI's 3000 series. (7M)

OR

Q. No.6 a) Draw the architecture of Xilinx XC 2000 CLB and explain it. (7M)
b) Explain the routing architecture of Xilinx XC 2000. (7M)

Section-IV

Q. No. 7 a) Explain different programming technologies used in CPLD and FPGA. (7M)

b) What are the features and applications of FPGA? (7M)

OR

Q. No. 8 a) what are difference between the ACT1 & ACT2 (7M)
b) What are differences between the ACT2 & ACT3 (7M)

Section-V

Q. No. 9 Implement the Excess 3 to BCD code converter Finite State Machine with PLA. (7M)

OR

Q. No. 10 Implement the BCD to Excess 3 code converter Finite State Machine with PROM. (7M)

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D6802 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
CPLD & FPGA Architectures Applications
(VLSI&ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

******

Section-I

Q. No. 1 a) Design a full subtractor circuit using ROM (7M)
b) Design a full adder circuit using PAL (7M)

OR

Q. No. 2 a) Draw and explain the architecture of ROM and EPROM. (7M)

b) Design a Half adder & Subtractor circuit using PAL (7M)

Section-II

Q. No. 3 a) Explain the applications of FPGAs (7M)
b) Explain the Programmable I/O blocks in FPGAs (7M)

OR

Q. No. 4 a) Explain generalized FPGA architecture with a neat block diagram. (7M)
b) Explain the Programmable Interconnects in FPGAs (7M)

Section-III

Q. No. 5 a) Draw the architecture of Xilinx XC 4000 CLB and explain it. (7M)
b) Explain the routing architecture of Xilinx XC 4000 (7M)

OR

Q. No.6 a) Draw the architecture of Xilinx XC 3000 CLB and explain it (7M)
b) Explain the routing architecture of Xilinx XC 2000 (7M)

Section-IV

Q. No. 7 a) Explain the Programming Technology of ACT1 (7M)
b) Explain different Programming Technologies used in CPLD &FPGA (7M)

OR

Q. No. 8 a) Explain the Device Architecture, The Actel ACT2 (7M)
b) Explain the Programming Technology of ACT3 (7M)

Section-V

Q. No. 9 a) Explain and draw the diagram with FPGA a Position Tracker for a Robot Manipulator. (7M)
b) Explain about a fast DMA controller (7M)

OR

Q. No. 10 Implement the Excess 3 to BCD code converter Finite State Machine with PLA. (14M)

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EMBEDDED SYSEM DESIGN
COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	CHAPTERS IN TEXT BOOK	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	ARM Systems Developer's Guides- Designing & Optimizing System Software	1,2	UNIT –I: ARM Architecture	Andrew N. Sloss, Dominic Symes, Chris Wright	Elsevier	2008
2	ARM Systems Developer's Guides	3	UNIT –II: ARM Programming Model – I	Andrew N. Sloss, Dominic Symes, Chris Wright	Elsevier	2008
3	ARM Systems Developer's Guides	4	UNIT –III: ARM Programming Model – II	Andrew N. Sloss, Dominic Symes, Chris Wright	Elsevier	2008
4	ARM Systems Developer's Guides	5,6	UNIT –IV: ARM Programming	Andrew N. Sloss, Dominic Symes, Chris Wright	Elsevier	2008
5	ARM Systems Developer's Guides	12	UNIT –V: Memory Management	Andrew N. Sloss, Dominic Symes, Chris Wright	Elsevier	2008

Code No: R15D9303

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech. I Semester Regular/supplementary Examinations, February 2017

Embedded System Design

(VLSI & ES, & SSP)

Roll No				N	3					

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

* * * * * *

SECTION - I

1. (a) Briefly explain the ARM register set organization in detail.
   (b) Discuss about evolution of the ARM processor families.

(OR)

2. (a) Write about ARM instruction set features differs from pure RISC characteristics
   (b) Explain the ARM processor modes and format of CPSR

SECTION – II

3. (a) Explain about different types of PSR and conditional instructions with suitable examples.
   (b) What is the function of Barrel shifter? Explain barrel shift related data processing instructions with an example.

(OR)

4. (a) Why the ARM instruction set is more suitable for the most the embedded applications? explain
   (b) Write about the ARM branch instructions in detail with suitable example.

SECTION – III

5. (a) Write the data processing instructions related to Thumb instruction set .
   (b) Discuss about the stack and software interrupt instructions in detail.

(OR)

6. (a) Briefly explain the Single-Register Load-Store Instructions
   (b) Explain about the ARM Thumb interworking in detail.

SECTION – IV

7. (a) Explain the scheduling for Load instructions in detail.
   (b) Discuss about the conditional execution of instructions with suitable example program

(OR)

8. Briefly Explain the Looping constructs with suitable example in each case

SECTION – V

9. Briefly explain the virtual memory concept in ARM processor with diagram.

(OR)

10. (a) Explain about two step page table method used in ARM MMU.
    (b) Write about caches and write buffer in ARM MMU.

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D9303 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Aug 2017
Embedded System design
(Common to VLSI & ES, & SSP)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing one Question from each section and each Question carries 15 marks.

* * * * * *

SECTION - I

1. (a) Briefly explain the importance of instruction pipeline depth in ARM processor
   (b) Draw the block diagram for ARM core data flow model and explain.

(OR)

2. (a) Discuss about interrupt vector table in ARM processor in detail.
   (b) Write about important features ARM 7 and ARM 9 family

SECTION – II

3. (a) Write about different types of load& store instructions with suitable examples.
   (b) Briefly explain the ARM branch instructions in detail with suitable examples

(OR)

4. (a) Discuss about the data processing instructions in ARM processor in detail
   (b) Explain the significance of different types of addressing modes in ARM.

SECTION – III

5. (a) Explain the importance of the Thumb instruction set in ARM processor.
   (b) Briefly explain the Multi-Register Load-Store Instructions

(OR)

6. (a) Explain about Stack Instructions and Software Interrupt Instructions.
   (b) Discuss about the Thumb instruction decoding with suitable example.

SECTION – IV

7. (a) Explain the optimization process in ARM programming.
   (b) Write short notes on register allocation and handling of unaligned data

(OR)

8. (a) Explain the bit manipulation instructions with suitable example
   (b) Write an assembly language program for finding highest number and smallest number in an array using loop instructions

SECTION – V

9. Briefly explain the ARM memory management unit using page tables and TLBs.

(OR)

10. (a) Discuss about procedure for the fast context switching in ARM
    (b) Write the different types of Access permissions of ARM?

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
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M. Tech – (VLSI & Embedded Systems)

Code No: R15D9303

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018
Embedded System Design
(VLSI& ES, & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

* * * * * *

SECTION - I

1. a) Explain the register organization of the ARM processor. (7M)
   (b) Write the various stages of instruction pipeline in ARM9. (8M)

(OR)

2. (a) Discuss the data flow in the ARM processor core. (7M)
   (b) Write about important features ARM 7 and ARM 9 family (8M)

SECTION – II

3. (a) Explain the addressing modes of the ARM with suitable examples. (7M)
   (b) Briefly explain the ARM data processing instructions in detail with suitable Examples. (8M)**(OR)**
4. (a) What are the unique features of the ARM instruction set? Explain. (7M)
   (b) Mention the importance of the load and store instructions in ARM with an Examples. (8M)

SECTION – III

5. (a) Discuss the software interrupt instructions used in ARM thumb instruction set . (8M)
   (b) Briefly explain usage of the registers in the ARM thumb mode (7M)

(OR)

6. Write the role of the stack operations in ARM thumb mode. (15M)

SECTION – IV

7. Briefly explain the functions, pointers and structures used in ARM c programming. (15M)

(OR)

8. (a) Write a ARM C code to find the numbers of continuous five 1's in given 6 bytes Data.(7M)
   (b) Write a ARM C code to sort 10 bytes stored in an array. (8M)

SECTION – V

9. Briefly explain the cache architecture and polices of the ARM processors. (15M)

(OR)

10. (a) Explain the implementation of the paging concept in ARM. (7M)
    (b) Write the short notes on context switching in ARM (8M)

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
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Code No: R17D9303

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Regular Examinations, Jan/Feb 2018
Embedded System Design
(VLSI& ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

* * * * * *

SECTION - I

1. (a) Write about ARM interrupts and vector table in detail. (8M)
   (b) Explain the ARM design philosophy. (6M)

(OR)

2. (a) Draw the CPSR format of ARM and explain with each bit in detail(7M)
   (b) Describe important features of the ARM families.(7M)

SECTION – II

3. (a) Write the conditional branch instructions in ARM and explain. (7M)
   (b) Discuss about the PSR instructions in ARM processor in detail. (7M)

(OR)

4. (a) Explain the load and store instructions in ARM processor. (7M)
   (b) Write the role of the barrel shifter in ARM instruction set and explain instructions related to it.(7M)

SECTION – III

5. (a) Explain how the code density will be improved by using ARM Thumb Instructions? (6M)
   (b) Discuss about the stack and software interrupt instructions in detail. (8M)

(OR)

6. (a) Write about single and multi register load and store instructions. (7M)
   (b) Discuss about the data processing instructions related to Thumb instruction set. (7M)

SECTION – IV

7. (a) Write a ARM C code to find out the factorial of given number. (5M)
   (b) Write about integer and floating point arithmetic instructions with suitable example. (9M)

(OR)

8. Discuss the various Looping constructs with suitable example in each case. (14M)

SECTION – V

9. Discuss about various methods involved in the handling of ARM MMU. (14M)

(OR)

10. (a) Describe the cache polices used in ARM . (7M)
    (b) Write a short note on access permission in ARM. (7M)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
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M. Tech – (VLSI & Embedded Systems)

Code No: R15D9303

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
Embedded System Design
(VLSI&ES & SSP)

R15

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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SECTION-I

1. (a). What is the arm design philosophy? 7M
   (b) Explain about the architecture of arm processor with neat block diagram? 8M

OR

2. (a) Write about the ARM programmer's model? 8M
   (b) Define pipelining and explain about the 3 stage pipelining in ARM in detail? 7M

SECTION-II

3. (a) Write about the Addressing modes in ARM? 8M
   (b) What is the importance of barrel shifter in data path and discuss the instructions related to the barrel shifter? 7M

OR

4. (a) Discuss about the Load and store instructions in ARM with an example? 8M
   (b) Explain about the conditional instructions in ARM with suitable example? 7M

SECTION-III

5. (a) Give details about the branch instructions in ARM? 7M
   (b) Explain about the difference between ARM and thumb instruction set with suitable example? 8M

OR

6. (a) Explain about the Single-Register and Multi Register Load-Store Instructions? 9M
   (b) Write about the software interrupt instructions? 6M

SECTION-IV

7. (a)Write a C program using function call and how is it compiled in ARM? 6M
   (b) Explain about the floating point number handling in ARM? 9M

OR

8. Write about pointer aliasing with an example and how to avoid pointer aliasing 15M

SECTION-V

9.(a) What is a virtual memory and how it works? 9M
   (b) Write short notes on flushing and cache memory? 6M

OR

10. (a) Explain about the ARM MMU? 10M
    (b) Write short notes context switch? 5M

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
Embedded System Design
(VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

* * * * * *

SECTION - I

11. (a) Explain ARM processor architecture revisions in detail. [7M]
    (b) Why the ARM processor is preferable for most of portable embedded systems? [7M]

(OR)

12. (a) Discuss the data flow in the ARM processor core. [7M]
    (b) Write about important features ARM 7 and ARM 9 family [7M]

SECTION – II

13. (a) Explain the addressing modes of the ARM with suitable examples [7M]
    (b) Discuss how the ARM processor instruction set is different from other processors. [7M]

(OR)

14. (a) What is the role of the conditional instructions in ARM programming [7M]
    (b) Mention the importance of the load and store instructions in ARM with an Examples [7M]

SECTION – III

15. (a) Explain the interrupt instructions in ARM processor. [7M]
    (b) Discuss the usage of the registers in the ARM thumb mode [7M]

(OR)

16. (a) Write the role of the stack operations in ARM thumb mode. [7M]
    (b) Write the important features of the ARM thumb instruction set. [7M]

SECTION – IV

17. Briefly explain the functions, pointers and structures used in ARM c programming. [14M]

(OR)

18. (a) Write a ARM C code to find the largest and smallest numbers in a 10 bytes of Data [7M]
    (b) Write a ARM C code to check given word is prime number or not. [7M]

SECTION – V

19. Briefly explain the cache architecture and polices of the ARM processors. [14M]

(OR)

20. (a) Explain the implementation of the paging concept in ARM [7M]
    (b) Write the short notes on context switching in ARM [7M]

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DIGITAL SYSTEM DESIGN
COURSE COVERAGE SUMMARY

S.No	TEXT BOOK TITLE	Units / Topics Covered	AUTHOR(S)	PUBLISHERS	EDITION
1	Fundamentals of Logic Design	I,II	Charles H. Roth	Cengage Learning	5th Ed.
2	Digital Systems Testing and Testable Design	IV	Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman	John Wiley & Sons Inc.	
3	Logic Design Theory	III,IV	N. N. Biswas	PHI	
4	Switching and Finite Automata Theory	V	Z. Kohavi	TMH	2nd Ed, 2001

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
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M. Tech – (VLSI & Embedded Systems)

Code No: R17D9309 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Regular Examinations, Jan/Feb 2018
Digital System Design
(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

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Section-I

Q. No. 1 a) Explain about the mealy sequential circuit design with relevant Block diagram. (7M)
b) An n-state machine is supplied with aperiodic input sequence whose period is 'p'. Prove that the output sequence must eventually become periodic, and find a bound for the period. (7M)

OR

Q. No. 2. Design a mealy sequential circuit that converts BCD digit to Excess-3 coded decimal digit.(14M)

Section-II

Q.No.3. Design a binary multiplier of 3bit using PLA. (14M)

Q.No.4. Design a 4×4 key pad layout. (14M)

	C0	C1	C2	C3
R3	1	2	3	A
R2	4	5	6	B
R1	7	8	9	C
R0	E	0	F	D

OR

scanner for the following keypad

Section-III

Q.No.5.a What are the components of an SM chart explain with suitable examples . (14M)

OR

Q.No.6. Design a SM Chart for Dice Game controller. (14M)

Section-IV

Q.No.7.a Write a short notes on single stuck at fault model. (7M)

b. Explain conventional methods of Fault diagnosis of combinational circuits. (7M)

OR

Q.No.8Find the test vectors to detect the fault signal x2 SA0 for the function f= x1* x2+x3*x4. (14M)

Section-V

Q.No.9.a.Write a short notes on homing experiment. (7M)

b. Explain the method of machine identification. (7M)

OR

Q.No.10 Explain the method of testing machines that have distinguishing sequences. (14M)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
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Code No: R17D9309 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
Digital System Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

Q. No. 1 .a) What is the difference between 'Mealy' and 'Moore' models of sequential machines? Explain using structural diagrams. (7M)

b) Explain the capabilities and limitation of FSM. (7M)

OR

Q. No. 2 Classify Hazards and implement the following Boolean function by Hazard free OR-AND network f= Σ (0,2,6,7) (14M)

SECTION-II

Q.No. 3.a. Derive the PLA Programming table for the combinational circuit that squares a 4-bit number.(7M)

b. Design a 32-bit adder circuit using PLD. (7M)

OR

Q.No.4. Design a scanner for telephone keypad using a PLD with state graph. (14M)

SECTION-III

Q.No.5.a Explain implementation of SM charts using microprogramming techniques. (7M)

b.Write a short notes on SM chart for DICE Game. (7M)

OR

Q.No.6. Design a SM Chart for Binary multiplier. (14M)

SECTION-IV

Q.No.7.a Explain about single stuck at fault model with an example. (7M)

b. Write short notes on D algorithm. (7M)

OR

Q.No.8. a. Explain Kohavi algorithm for fault testing and modeling. (7M)

Explain the different path sensitization techniques. (7M)

SECTION-V

Q.No.9.a. Explain the method of machine identification. (7M)

b. What is distinguishing tree. Explain its significance in testing of sequential circuits. (7M)

OR

Q.No.10 Explain the different state-identification experiments and testing of sequential circuits. (14M)

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	CMOS Analog Circuit Design	UNIT –I TO UNIT-V	Philip E. Allen and Douglas R. Holberg	Oxford University Press, International	Second Edition/Indian Edition, 2010.
2	Analysis and Design of Analog Integrated Circuits-	UNIT -I: MOS Devices and Modeling UNIT -II: Analog CMOS Sub-Circuits	Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer,	Wiley India	Fifth Edition, 2010.
3	Analog Integrated Circuit Design	UNIT -II: Analog CMOS Sub-Circuits UNIT -III: CMOS Amplifiers UNIT -IV: CMOS Operational Amplifiers	David A. Johns, Ken Martin	Wiley Student Edn,	2013

R15

Code No: R15D6805

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech. I Semester Regular/supplementary Examinations, February 2017

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No			N	3						

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

* * * * * *

SECTION - I

1 a) Explain the complete large signal model for the MOS transistor
b) Explain the Computer Simulation models

(OR)

2 a) Explain the role of passive components in the fabrication of MOS devices.
b) Explain the small signal model for the MOS transistor

SECTION – II

3 a) Draw and explain the circuit of current mirror with beta helper .
b) Explain in detail the design and operation cascode current Mirror.

(OR)

4 a) Explain the hierarchy of analog circuits for an operational amplifier.
b) Write a short note on how MOS switch, Current Sinks.

SECTION – III

5. Draw and explain about CMOS differential amplifiers in detail?

(OR)

6) Draw and explain about CMOS cascode amplifiers in detail?

SECTION – IV

7) Explain about in detail about Cascode op-amp?

(OR)

8) Explain the measurement techniques of op-amp in detail?

SECTION – V

9) a) What is a comparator? List the important characteristics of the comparator.
b) Explain about two stage open loop comparators?

(OR)

10) a) Explain about different open loop comparators with neat circuit diagrams.
b) Explain about discrete time comparator?

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6805 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Aug 2017
CMOS Analog Integrated Circuit Design
(VLSI & ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing one Question from each section and each Question carries 15 marks.

* * * * * *

SECTION - I

1 a) Explain MOS Semiconductor fabrication process.
b) Explain the structure of n-channel and p-channel MOS Transistor fabricated using n-well local oxidation silicon.

(OR)

2 a) Explain the role of passive components in the fabrication of MOS devices.
b) Explain the complete large signal model for the MOS transistor

SECTION – II

3 a) Draw the circuit of n-channel current mirror and explain its characteristics.
b) Explain in detail the design and operation of Wilson Current Mirror.

(OR)

4 a) Explain the hierarchy of analog circuits for an operational amplifier.
b) Write a short note on how MOS diode acts as Active Resistor, Current Sink and Source.

SECTION – III

5 a) Why is emitter resistor RE replaced by a constant current bias circuit in differential amplifier stage of an op-AMP?
b) Draw and explain CMOS inverter circuit.

(OR)

6) Draw and explain about CMOS current amplifiers in detail?

SECTION – IV

7) Discuss in detail the compensation of OP amp that makes it completely independent of process and temperature variations.

(OR)

8) Explain the design issues of CMOS op-amp in detail?

SECTION – V

9) a) What is a comparator? List the important characteristics of the comparator.
b) Explain different types of comparators with neat circuit diagrams.

(OR)

10) a) Explain about how to improve the performance of open loop comparators?
b) Explain about discrete time comparators?

* * * * * * * * * *

Code No: R15D6805

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018
CMOS Analog Integrated Circuit Design
(VLSI& ES)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

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Section-I

1. a. Draw the Large-signal model for the MOS Transistor and explain. 8M
   b. Explain about computer simulation model. 7M

OR

2.a Discuss about the Passive Components of the MOS transistor. 8M
b. Draw the small-signal model for the MOS transistor and explain. 7M

Section-II

3.a Draw the given simplest forms of the current mirror for the following i) Bipolar version of current mirror ii) MOS version of the current mirror. 8M
b. Discuss the influence of the capacitance in MOS switch. 7M

OR

4.a Draw the circuit diagram of MOSFET switch and discuss the salient features? 8M
b.Discuss the effects on characterization of MOSFET Sinks and Sources. 7M

Section-III

5.a What are the Characteristics of an amplifier and name the types of amplifiers, enumerate the input and output resistances. 8M
b. Design of a CMOS Differential amplifier with a Current Mirror Load ? 7M

OR

6.a Draw the circuit diagram of voltage driven cascode amplifier also discuss Large-Signal Characteristics of the Cascode Amplifier. 8M
b. Briefly explain the differential amplifiers. 7M

Section-IV

7.Explain about the design of Two-stage op-amps and the key design issues of it?15M

OR

8.Explain the various Measurement technologies of Op-amp. 15M

Section-V

9.a.What is a comparator and types and static characteristic of a comparator? 8M
b. Compare infinite and finite gain comparator. 7M

OR

10.a.Draw the Two-Stage Comparator with Increased Speed and write the salient features. 8M
b. Draw the circuit diagram of folded cascade comparator? 7M

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
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M. Tech – (VLSI & Embedded Systems)

R15

Code No: R15D6805

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
CMOS Analog Integrated Circuit Design
(VLSI&ES)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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SECTION-I

1.a What do you mean by sub threshold MOS model, explain? [8M]
b. Draw the small-signal model for the MOS transistor. Briefly explain each component in that? [7M]

OR

2. a.Name the types of resistors and capacitors in analog design for CMOS VLSI systems and the factors effecting accuracy? [8M]
b. Explain the Large-signal model for the MOS Transistor. [7M]

SECTION-II

3.a Discuss the influence of the ON resistance in MOS switch. [8M]
b. Explain in details the MOS cascode current mirror with necessary equations. [7M]

OR

4.a Write the analytical expressions to approximate charge injection/clock feed through. [8M]
b. Explain about the Bipolar simple current mirror with degeneration helper with necessary equation. [7M]

SECTION-III

5.a Draw the circuit diagram of the noise model of inverting amplifiers and summarize the voltage gain and output resistance under various loads. [8M]
b. Explain the Voltage Transfer Characteristic of the Differential Amplifier with current mirror load? [7M]

OR

6.a Draw the circuit diagram of voltage driven common gate amplifier also discuss Small Signal Performance of the Common Gate Amplifier. [8M]
b. What are the Characteristics of an amplifier and Name the types of amplifiers. [7M]

SECTION-IV

7. Explain the PSRR of the two-stage, Miller compensated op amp? [15M]

OR

8. What are the various cascode schemes of CMOS Op-amps and explain any one? [15M]

SECTION-V

9.a. What is a comparator and types and static characteristic of a comparator? [8M]
b. Compare infinite and finite gain comparator. [7M]

OR

10a. Draw the circuit diagram of two pole comparator and write the salient features. [8M]
b. Draw the circuit diagram of folded cascade comparator? [7M]

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Digital Integrated Circuit Design	UNIT –I: MOS Design	Ken Martin	Oxford University Press	2011
2	Digital Integrated Circuit Design	UNIT –II: Combinational MOS Logic Circuits	Ken Martin	Oxford University Press	2011
3	Digital Integrated Circuit Design	UNIT –III: Sequential MOS Logic Circuits	Ken Martin	Oxford University Press	2011
4	CMOS Digital Integrated Circuits Analysis and Design	UNIT –IV: Dynamic Logic Circuits	Sung-Mo Kang, Yusuf Leblebici	TMH	3 rd Ed., 2011
5	CMOS Digital Integrated Circuits Analysis and Design	UNIT –V: Semiconductor Memories	Sung-Mo Kang, Yusuf Leblebici	TMH	23 rd Ed., 011

Code No: R15D6807 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech. I Semester Regular/supplementary Examinations, February 2017

CMOS Digital Integrated Circuit Design

(VLSI & ES)

Roll No			N	3						

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks * * * * * *

SECTION - I

1. Define Rise time and Fall time. Derive Rise time and Fall time equations for CMOS inverter and pseudo-nmos NOR gate [15]

(Or)

2. (a) What is Transistor equivalency? Explain.
   (b) Design Exclusive-OR using pass-transistor logic. [7+8]

SECTION – II

3. (a) Explain the propagation delay and power consumption issues of CMOS gate.
   (b) Explain how MOS inverters connected in cascade can drive large capacitive loads. [8+7]

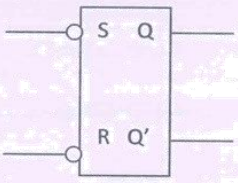
(Or)

4. (a) Realize boolean expression Z=AB+C using differential CMOS gates
   (b) Draw the circuit of NMOS OAI gate and write the function table. [8 +7]

.SECTION – III

5. (a) Design a gate level design to implement the truth table shown in fig below.

S	R	Q	Q'
0	1	1	0
1	0	0	1
1	1	Q	Q'



(b) Write about sequential logic and depict the classification and critical elements of sequential system. [10+5]

(Or)

6. (a)Explain about CMOS SR latch circuit based on NOR2 gates with its truth table
   (b) Sketch AOI based implementation of the clocked NOR based SR latch circuit. [10+5]

SECTION – IV

7. Explain in detail synchronous dynamic circuit techniques. [15]

(Or)

8. (a) Explain about Domino CMOS logic.
   (b) With necessary equations explain voltage bootstrapping in CMOS circuits.[8+7]

SECTION – V

9. (a) Explain the NAND gate flash memory with neat sketch.
   (b) Compare SRAM and DRAM [8+7]

(Or)

10. (a) Explain in detail about leakage currents in SRAM cells.
    (b) With the help of timing waveforms, explain read and write operations of SRAM [8+7]

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

R15

Code No: R15D6807

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Aug 2017
CMOS Digital Integrated Circuit design
(VLSI & ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing one Question from each section and each Question carries 15 marks.

* * * * * *

SECTION - I

1. Determine Pull-up to pull-down ratio for NMOS inverter. Explain the criteria for voltage threshold for high level and low level in NMOS inverter characteristics. [15]

(or)

2. (a) Explain the following terms with reference to CMOS logic.
   i Logic Levels
   ii Noise margin
   iii Power supply rails
   iv Propagation delay
   (b) What is the difference between transmission time and propagation delay? Explain these two parameters with reference to CMOS logic. [8+7]

SECTION – II

3. (a) Realize Boolean expressions Z=AB+C using differential CMOS gates.
   (b) Draw the circuit of NMOS OAI gate and write the function table. [8 +7]

(or)

4. (a) Explain how MOS inverters connected in cascade can drive large capacitive loads.
   (b) Explain the operation of a CMOS full adder circuit with neat schematic. [8+7]

.

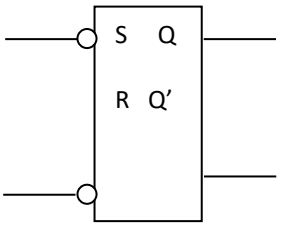
SECTION – III

5. Explain the operation of CMOS D-Latch and CMOS negative edge triggered master slave DFF. [15]

(Or)

6. (a) Design a gate level design to implement the truth table shown in Fig below.

S	R	Q	Q'
0	1	1	0
1	0	0	1
1	1	Q	Q'



(b) Explain the static behavior of two inverter basic bistable element. [10+5]

SECTION – IV

. 7. Explain dynamic CMOS circuit and synchronous dynamic circuit techniques. [15]

(Or)

8. (a) Explain voltage bootstrapping in CMOS circuit with necessary equations.
(b) Write about high performance dynamic CMOS circuits [8+7]

SECTION – V

9. (a) Explain the NOR gate flash memory with neat sketch.
(b) Compare SRAM and DRAM [8+7]

(Or)

10. (a) Explain the internal structure of 64K X 1 DRAM. With the help of timing waveforms discuss DRAM access.
(b) Explain the necessity of two dimensional decoding mechanisms in memories.

[7 +8]

* * * * * * * * * *

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6807 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018
CMOS Digital Integrated Circuit Design
(VLSI& ES)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

****

Section-I

1. a. What do you mean by transistor equivalency and explain how it is useful in design of MOS circuits. (7M)
b. What are the features of pseudo-NMOS logic and draw the circuit diagram of pseudo-NMOS XOR gate? (8M)

OR

2.a Determine the pull-up to pull-down ratio for an NMOS inverter. (8M)
b. Explain and derive the necessary DC region equations of a CMOS inverter. (7M)

Section-II

3. a. Explain the procedure to design an adder circuit using CMOS logic. (8M)
b. Explain the voltage transfer characteristics of a CMOS inverter with a neat diagram. (7M)

OR

4.a How the MOS inverters connected in cascade can drive large capacitive loads? Explain. (8M)
b. Write short notes on transmission gates with the relevant circuits. (7M)

Section-III

5.a. Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table. (8M)
b. Differentiate between static and dynamic latches. (7M)

OR

6.a Draw the circuit diagram of CMOS negative edge trigged master slave D FF and explain the features?(8M)
b. Draw the circuit diagram of CMOS SR latch using NOR gates and operating modes? (7M)

Section-IV

7. a. Explain dynamic boot strapping. (8M)
b. Explain the speed and power dissipation in dynamic CMOS logic.(7M)

OR

8.a. What are the various issues in CMOS dynamic logic design? Explain anyone with a neat sketch. (8M)
b. What is a dynamic gate and discuss its properties. (7M)

Section-V

9.a What are the types of DRAM? Explain any one. (8M)
b. Describe the leakage currents in DRAM cell. (7M)

OR

10.)a. Compare the SRAM and DRAM. (8M)
b Write notes on Ferro electric Random Access Memory (FRAM). (7M)

R17

Code No: R17D6807

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018
CMOS Digital Integrated Circuit Design
(VLSI& ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

Section-I

1. a. What do you mean by transistor equivalency and explain how it is useful in design of MOS circuits. (7M)

b. What are the features of pseudo-NMOS logic and draw the circuit diagram of pseudo-NMOS XOR gate? (7M)

OR

2.a Determine the pull-up to pull-down ratio for an NMOS inverter. (7M)
b. Explain and derive the necessary DC region equations of a CMOS inverter. (7M)

Section-II

3. a. Explain the procedure to design an adder circuit using CMOS logic. (7M)
b. Explain the voltage transfer characteristics of a CMOS inverter with a neat diagram. (7M)

OR

4.a How the MOS inverters connected in cascade can drive large capacitive loads? Explain. (7M)
b. Write short notes on transmission gates with the relevant circuits. (7M)

Section-III

5.a. Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table. (7M)
b. Differentiate between static and dynamic latches. (7M)

OR

6.a Draw the circuit diagram of CMOS negative edge trigged master slave D FF and explain the features? (7M)
b. Draw the circuit diagram of CMOS SR latch using NOR gates and operating modes? (7M)

Section-IV

7. a. Explain dynamic boot strapping. (7M)
b. Explain the speed and power dissipation in dynamic CMOS logic.(7M)

OR

8.a. What are the various issues in CMOS dynamic logic design? Explain anyone with a neat sketch. (7M)
b. What is a dynamic gate and discuss its properties. (7M)

Section-V

9.a What are the types of DRAM? Explain any one. (7M)
b. Describe the leakage currents in DRAM cell. (7M)

OR

10.)a. Compare the SRAM and DRAM. (7M)
b Write notes on Ferro electric Random Access Memory (FRAM). (7M)

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6807

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
CMOS Digital Integrated Circuit Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

******

SECTION-I

1.a Explain the DC noise margin of CMOS logic. (8M)
b. Explain the factors to be considered while choosing transistor sizes? (7M)

OR

2.a Determine the pull-up to pull-down ratio for an NMOS inverter. (8M)
b. What are the Features of pseudo-NMOS logic and draw the circuit diagram of pseudo-NMOS XOR gate? (7M)

SECTION-II

3.a. Bring out the differences between Pass Transistor logic and transmission gate logic. (8M)
b. Explain the propagation delay and power consumption issues of CMOS gate. (7M)

OR

4. a Design and explain the operation of 2 input NMOS NAND. (8M)
b. Draw the CMOS full adder circuit and explain its operation. (7M)

SECTION-III

5.a Discuss the CMOS two inverter bistable element? (8M)
b. What is the drawback of SR latch and it can be overcome by using feedbacks, draw the circuit diagram of CMOS AOI based JK latch? (7M)

OR

6.a Draw the circuit diagram of Schmitt trigger circuit and explain its operation? (8M)
b. Draw the circuit diagram of CMOS SR latch using NOR gates and operating modes? (7M)

SECTION-IV

7. a. Explain dynamic boot strapping. (8M)
b. Explain the speed and power dissipation in dynamic CMOS logic. (7M)

OR

8.a. What is cascading problem in dynamic CMOS logic and it can be overcome? (8M)
b. Discuss NORA CMOS logic circuit with an example? (7M)

SECTION-V

9.a Write about the leakage currents in SRAM. (8M)
b Explain NOR flash memory? (7M)

OR

10.a Compare the SRAM and DRAM. (8M)
b Write notes on Ferro electric Random Access Memory (FRAM). (7M)

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D6807 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
CMOS Digital Integrated Circuit Design
(VLSI&ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1a) What are the advantages of pseudo – nMOS logic? Draw the circuit diagram of pseudo – NMOS NOR gate and explain its operation. (8M)
b) What do you mean by transistor equivalency and explain how it is useful in design of MOS circuits (6M)

(OR)

2a) Determine the pull-up to pull- down ratio for NMOS inverter. (7M)
b) Design an inverter using (i) NMOS; (ii) CMOS and (iii) pseudo NMOS. Compare and Explain the characteristics of above designs. (7M)

SECTION-II

3a) Design and explain the operation of 2 input NMOS NOR Gate. (7M)
b) Explain the concept of charge storage and charge leakage associated with pass transistor logic. (7M)

(OR)

4a) Realize NMOS complex logic gates using the Boolean function Z=A(D+C)+BE (7M)
b) Design full adder using transmission logic and explain its operation. (7M)

SECTION-III

5a) Explain the behavior of bistable elements. (7M)
b) Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table. (7M) (OR)

6a) Draw the Circuit diagram of a CMOS bi-stable element and explain the output time domain behavior . (7M)
b) Draw the D latch by using CMOS logic and explain its operation in detail. (7M)

SECTION-IV

7a) Design and explain the high performance dynamic CMOS circuits (7M)
b) With an example, briefly explain about the principle of voltage bootstrapping (7M)

(OR)

8a) What are the various issues in CMOS dynamic logic design? Explain anyone with a neat sketch. (7M)
b) Bring out the differences between Pass Transistor logic and transmission gate logic. (7M)

SECTION-V

9a) What are the types of DRAM? Explain any one. (7M)
b) Draw memory architecture. Write about the leakage currents in SRAM. (7M)

(OR)

10a) Draw a circuit diagram for 6 – transistor SRAM cell and explain how it stores data? (7M)
b) Explain NOR and NAND flash memory. (7M)

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17DEC51 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Regular Examinations, Jan/Feb 2018
Embedded Systems Programming
(VLSI& ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

SECTION-I

1. Explain the use of semaphore in LINUX operating system with an example(14M)

(OR)

2. Explain the memory management in LINUX operating ssytem. (14M)

SECTION-II

3. Define RTOS? Explain Hard and soft real time system (14M)

(OR)

4. a) Explain the differences between general purpose operating system and RTOS(7M)
   b) What are the disadvantages of RTOS? (7M)

SECTION-III

5. Explain basic issues in selecting a RTOS? Explain.(14M)

(OR)

6. Explain the interprocess communications in RTOS. (14M)

SECTION-IV

7. What is Shared data problem? Explain with an example how semaphore used to solve the problem(14M)

(OR)

8. What are device drivers? Explain device drivers functions in RTOS(14M)

SECTION-V

9. Explain the build process for the embedded systems. (14M).

(OR)

10. Explain different laboratory tools used to test embedded boards(14M)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17DEC51 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018
Embedded Systems Programming
(VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

11. Explain in detail file management in LINUX operating system (14M)

(OR)

12. Explain the interfacing of USB device drivers to LINUX operating system (14M)

SECTION-II

13. What is an Interrupt? Explain interrupt routine in RTOS Environment (14M)

(OR)

14. a) Explain the architecture of an RTOS(8M)
    b) What are the advantages of RTOS? (6M)

SECTION-III

15. What is a POSIX standard in RTOS? Explain.(14M)

(OR)

16. Explain Xenomai basics (14M)

SECTION-IV

17. What is a Task in RTOS? Explain Message Queue in RTOS(14M)

(OR)

18. Write short notes on Pipes and signals (7+7=14M)

SECTION-V

19. Explain Tool chain for building embedded software (14M).

(OR)

20. Explain the porting of RTOS to a target board.(14M)

****

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

I YEAR II SEMESTER

COURSE COVERAGE SUMMARY & QUESTION BANK

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

EMBEDDED REAL TIME OPERATING SYSTEMS

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Advanced UNIX Programming	UNIT – I: Introduction	Richard Stevens		2000
2	Real Time Concepts for Embedded Systems	UNIT - II: Real Time Operating Systems	Qing Li	Elsevier	2011
3	Real Time Concepts for Embedded Systems	III: Objects, Services and I/O IV: Exceptions, Interrupts and Timers V: Case Studies of RTOS	Qing Li	Elsevier	2011

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D9314 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Regular Examinations, Aug 2017
Embedded RTOS
(Common to CSE, VLSI& ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

****

Section-I

1. Explain the UNIX file I/O commands.

OR

2. Explain the process control commands with examples

Section- II

3. What is meant by "Tasks" in RTOS? Explain in detail about task scheduler

OR

4. Write notes on "Semaphores" and "Mutex" in connection with embedded RTOS.

Section- III

5. Define and briefly explain the following related to embedded RTOS.
   a) Message queues
   b) Event registers And Pipes

OR

6. Explain the concept of I/O sub system

Section- IV

7. Explain interrupt service routines related to embedded RTOS.

OR

8. Explain the real time clocks and programmable timers

Section- V

9. Write notes on
   a. Embedded Linux b. RT LINUX

OR

10. Write a short note on
    a) Vx works b) Android OS

****

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D9314 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Supplementary Examinations, July/Aug 2018
Embedded RTOS
(CSE, VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

SECTION-I

1. a) Write the function of the following: [5*3=15M]
   i)lseek ii) vfork iii) waitpid iv) pend v) fwrite

(OR)

2. a) Write the function of the following: [5*3=15M]
   i)open ii) create iii) close iv) exec v) OSSemPost ( )

SECTION-II

3. a) Explain Task and task states? [10M]
   b) List out the various Key Characteristics of an RTOS. [5M]

(OR)

4. a) Discuss about Message Queue. [7M]
   b) Discuss about Scheduling Algorithms. [8M]

SECTION-III

5. How do you create, remove, open, close, read, write and IO control a device using RTOS functions? Take an example of a pipe delivering an IO stream from a network device. [15M]

(OR)

6. a) Explain select operation is allowed on pipes. [8M]
   b) List out various Event Registers? Explain it? [7M]

SECTION-IV

7. a) Nested Exceptions and Stack Overflow? [7M]
   b) Explain nature of Spurious Interrupts. [8M]

(OR)

8. a) Explain about programmable timers and soft timers. [8M]
   b) Real-Time Clocks and System Clocks. [7M]

SECTION-V

9. Explain how to achieve communication between a process running in Linux and a process running in RT Linux. [15M]

(OR)

10. Explain the case study of coding for sending application layer byte stream on a TCP/IP network using RTOS Vx works. [15M]

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D9314 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Regular Examinations, July/Aug 2018
Embedded Real Time Operating Systems
(VLSI & ES & SSP)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

Section-I

Q. No. 1 a) Write a program illustrates the use of fork ( ) function call. [7M]
b) Write short notes on process commands. [7M]

OR

Q. No. 2 a) Explain the goals of services. [7M]
b) Explain the use of Semaphore and write the program. [7M]

Section-II

Q. No. 3 a) Explain the memory management in RTOS. [10M]
b) List the basic design principles in RTOS. [4M]

OR

Q. No. 4 a) Explain the types of RTOS programming. [7M]
b) Explain the system level functions of MicroC/ OS-II in RTOS. [7M]

Section-III

Q. No. 5 a) Draw the basic system of ACVM and explain the system specifications in detail. [7M]
Explain about task and task states with neat diagram. [7M]

OR

Q. No.6 a) Describe about Event Registers. [7M]
b) Explain basic input and out sub systems. [7M]

Section-IV

Q. No. 7 a) Explain the following functional parameters of real time systems. [9M]
i) Pre-emptivity of jobs ii)Criticality of jobs iii)Laxity type and Laxity function
b) Illustrate the weighted round robin approach used in Real time systems with an example and Relevantf figures

OR

Q. No. 8 a) Interpret the need of RTOS in a Real Time System? List and explain the important features and services of real time operating systems. [7M]
b) Explain how RTOS can used for implementing the control system applications with examples. [7M]

Section-V

Q. No. 9 a) Draw and explain ACC Hardware Architecture. [7M]
b) Discuss operating system software. [7M]

OR

Q. No. 10 a) Explain the architecture of Android OS. [7M]
b) Discuss OS security issues. [7M]

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

CMOS MIXED SIGNAL CIRCUIT DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Design of Analog CMOS Integrated Circuits-	UNIT -I: Switched Capacitor Circuits	Behzad Razavi	TMH Edition	2002
2	Design of Analog CMOS Integrated Circuits	UNIT -II: Phased Lock Loop (PLL):	Behzad Razavi	TMH Edition	2002
3	CMOS Analog Circuit Design	UNIT -III: Data Converter Fundamentals	Philip E. Allen and Douglas R. Holberg,	Oxford University Press,International	Second Edition/Indian Edition, 2010.
4	Analog Integrated Circuit Design-	UNIT -IV: Nyquist Rate A/D Converters UNIT -V: Oversampling Converters	David A. Johns,Ken Martin,	Wiley Student Edition	2013

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6811

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M. Tech I Year - II Semester Regular Examinations, Aug 2017
CMOS Mixed Signal Circuit Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

Section-I

1. a) What is switched capacitor? What is its significance in the CMOS technology? [7M]
   b) Draw the basic circuit of a switched capacitor, its equivalent circuit, explain its operation and Derive its equivalent resistor value [8M]

OR

2.a) Derive an integrator using switched capacitor circuit. [7M]
   b) What are biquad filters? Explain about the two switched capacitor biquad realizations. [8M]

Section-II

3.a) With the help of necessary waveforms, explain about the non-ideal effects in PLLs. [7M]
   b) Explain the Jitter in PLLs and delay locked loops and basics of PLL topology [8M]

OR

4.a) Explain the basic charge pump PLL and non-ideal effects in PLLs. [8M]
   b) What are the applications of PLL? [7M]

Section-III

5.a) Give the classification of ADC architectures based on the conversion rate. [8M]
   b) Write about hybrid converters. [7M]

OR

6.a) Explain about deterministic approach and statistic approach of quantization noise in data Converters. [8M]
   b) What are the dynamic characteristics that influence the performance of DACs? [7M]

Section-IV

7.a) What is time interleaving? Explain the operation of a time interleaved ADC. [8M]
   b) What is a Successive approximation converter? Discuss the working of Successive Approximation A/D Converter [7M]

OR

8.a) Draw the block diagram of a D-A converter and explain it. [8M]
   b)Explain pipelined A-D converter?. [7M]

Section-V

9.a) Discuss about Delta-Sigma DAC. [7M]
   b) Explain the block diagram of second order Delta-Sigma modulator. [8M]

OR

10.a) Distinguish oversampling without noise shaping and with noise shaping. [8M]
   b) Explain Noise shaping modulators? [7M]

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
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M. Tech – (VLSI & Embedded Systems)

Code No: R15D6811

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester supplementary Examinations, Jan/Feb 2018
CMOS Mixed Signal Circuit Design
(VLSI&ES)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

.Section-I

1. a) Explain the non-ideal characteristics of a switched capacitor integrator. [8M]
   b) Explain the techniques that are adopted in a switched capacitor integrator circuit to minimize charge injection issues. [7M]

OR

2.a) Draw the basic circuit of a switched capacitor, its equivalent circuit , explain its operation and derive its equivalent resistor value. [10 M]
   b) For the above circuit if clock frequency is 100kHz, find the capacitor value that will emulate 1M ohm resistor. [5M]

Section-II

3.a) Explain the basic charge pump PLL and non-ideal effects in PLLs. [8M]
   b) Explain the Jitter in PLLs and delay locked loops. [7 M]

OR

4.a) With the help of necessary waveforms, explain about the non-ideal effects in PLLs. [8M]
   b) Explain about the basic charge pump PLL with a neat figure. [7M]

Section-III

5.a). Explain Binary Scaled converters. [7M]
   b) Write about hybrid converters. [8M]

OR

6.a) Explain about deterministic approach and statistic approach of quantization noise in data converters. [8M]
   b) Design a decoder based DAC with a detailed explanation.[7M]

Section-IV

7.a) Mention all kinds of medium speed and high speed ADC and explain the operation of a multiple- bit pipeline ADC. [8M]
   b) What is a Flash converter? Discuss the working of a 3-bit Flash A/D Converter. [7M]

OR

8.a) Draw the block diagram of a D-A converter in signal processing applications. [8M]
   b) Explain the static and dynamic characteristics of DAC. [7M]

Section-V

9.a) Discuss about Delta-Sigma ADC. [7M]
   b) Explain the block diagram of second order Delta-Sigma modulator. [8 M]

OR

10.a) Design a high-speed noise-shaping converter using a cascaded modulator. [7M]
   b) Explain Interpolating Filters and Decimating Filters. [8M]

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6811 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Supplementary Examinations, July/Aug 2018
CMOS Mixed Signal Circuit Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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SECTION - I

1.	a)	Describe the basic building blocks of switched capacitor circuits and list their desirable characteristics	8M
	b)	What is the equivalent resistance of a 5 pF capacitance sampled at a clock frequency of 100 kHz?	7M
		OR	
2.	a)	With the help of a neat circuit diagram, explain the operation of parasitic-sensitive and parasitic-insensitive switched capacitor integrator	8M
	b)	Derive the active RC realization of a continuous time biquad filter with the help of signal flow graph realization.	7M

SECTION – II

3.	a)	Draw the block diagram of a basic PLL and explain the input-output characteristics of each block.	8M
	b)	Explain the use of phase locked loops in clock skew and jitter reduction	7M
		OR	
4.	a)	With the help of neat waveforms, explain the operation of phase-frequency detector and derive a possible implementation	8M
	b)	Derive the transfer function of a Type-I PLL and describe the tradeoffs	7M

SECTION – III

5.	a)	Describe the input-out description of an ideal D/A and A/D converter with appropriate mathematical equations and input-output plots.	8M
	b)	With a neat sketch, explain the thermometer code converter and mention its applications	7M
		OR	
6.	a)	Describe the deterministic and stochastic modeling of quantization noise in data conversion systems.	8M
	b)	Draw the circuit diagram and explain the operation of binary –weighted resistor converters	7M

SECTION – IV

7.	a)	What is the fundamental advantage of a pipelined A/D converter? Explain the signal flow and operation of one bit per stage pipelined converter	8M
	b)	Classify the different A/D converter architectures and comment on their speed and accuracy.	7M
		OR	
8.	a)	With the help of a flow chart and block diagram, explain the operation of a successive approximation A/D converter	8M
	b)	Explain the issues in the design of flash A/D converter	7M

SECTION – V

9.	a)	With the help of a neat block diagram, describe the system architecture of Delta-Sigma A/D Converters	8M
	b)	Distinguish between oversampling without and with noise shaping	7M
		OR	
10.	a)	Explain the use of decimation and interpolation filters in oversampling A/D converters	8M
	b)	Derive the switched-capacitor realization of a First-Order A/D Converter .	7M

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D6811

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Regular Examinations, July/Aug 2018
CMOS Mixed Signal Circuit Design
(VLSI &ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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Section-I

Q. No. 1 What are the basic building blocks of switched capacitors and explain about each of them.[14M]

OR

Q. No. 2 Explain the operation of switched capacitor integrators first order filters. [14M]

Section-II

Q. No. 3 a) List out the various applications of the PPL and explain about any two of them. [8M]
b) Write in detail about the phase/frequency detector. [6M]

OR

Q. No. 4 a) Explain the operation of basic charge pump in PLL? [7M]
b) Explain the operation of Jitter in PLL [7M]

Section-III

Q. No. 5 what are the various Nyquist rate D/A converters and explain in detail about any two of them? [14M]

OR

Q. No.6 a) Explain the operation of binary scaled converters. [7M]
b) Explain the operation of Thermometer-code converters. [7M]

Section-IV

Q. No. 7 a) What is flash converter? Explain its 3 bit flash type A-D converter. [7M]
b) Explain the operation of successive – approximation converters. [7M]

OR

Q. No. 8 a) Discuss the advantages and disadvantages of using a dual slope over a single slope ADC.[7M]
b) Explain the Data Converter Fundamentals. [7M]

Section-V

Q. No. 9 with neat block diagram, describe the operation of multistage decimation filter operation. [14M]

OR

Q. No. 10 a) Explain the Delta sigma modulators with multibit quantizers. [7M]
b) Explain the principle of interpolation filters**.[7**M]

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

LOW POWER VLSI DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Low-Voltage, Low-Power VLSI Subsystems	I,II	Kiat-Seng Yeo, Kaushik Roy	TMH Professional Engineering	TMH
2	Introduction to VLSI Systems: A Logic, Circuit and System Perspective	I,II	Ming-BO Lin	CRC Press	2011
3	CMOS Digital Integrated Circuits – Analysis and Design	III,IV,V	Sung-Mo Kang, Yusuf Leblebici,	TMH	2011

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6812

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Regular Examinations, Aug 2017
Low Power VLSI design
(VLSI&ES)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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Section-I

Q. No. 1 a) Explain static and dynamic power dissipation in CMOS inverter? 7M
b) What is short channel effect? 8M

OR

Q. No. 2 a) Explain DIBL, velocity saturation and hot electron effect? 9M
b) What is Glitching power and leakage power in CMOS circuits? 6M

Section-II

Q. No. 3 a) Explain System-Level measures for reduction of Switched Capacitance? 6M
b) Explain Multiple-Threshold CMOS Circuit? 9M

OR

Q. No. 4 a) What are different Low power design approaches? 5M
b) How does power and delay parameter gets affected when the voltage is scaled? 5M
c) What is the effect of Threshold voltage on circuits? 5M

Section-III

Q. No. 5 a) Design transmission gate full adder circuit diagrams? 7M
b) Explain different low-power low-voltage logic styles in adder design? 8M

OR

Q. No.6 a) Differentiate between carry save adder, carry skip adder and carry look-Ahead adders? 9M
b) Write the sum expression reusing carryout term? 3M
c) Draw the full adder logic diagram using half adder? 3M

Section-IV

Q. No. 7 a) Explain 4x4 bit Baugh-Wooley Multiplier with neat block diagram and its operation? 15M

OR

Q. No. 8 a) Explain Modified Booth algorithm to multiply 16bit numbers? 15M

Section-V

Q. No. 9 a) Draw the basic block diagram of DRAM architecture? 5M
b) Explain static and dynamic decoder used in memory circuits? 8M
c) Draw the circuit diagram of 7T SRAM? 2M

OR

Q. No. 10 a) Explain read and write cycle of SRAM with timing diagram? 3M
b) What are the future developments in ROM, SRAM and DRAM? 12M

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D6812 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Regular Examinations, July/Aug 2018
Low Power VLSI design
(VLSI &ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

Q. No. 1 a) What are the various issues involved in low power VLSI Design? Explain (6M)
b) Explain about Sub-threshold leakage in a MOS transistor (8M)

OR

Q. No. 2 What is short channel effect and can you elaborate the short channel effects? (14M)

SECTION-II

Q. No. 3 a) With necessary schematics explain the concept of MTCMOS technique (6M)
b) Can you distinguish between pipelining and parallel processing approaches with suitable examples? (8M)

OR

Q. No. 4 a) How could you minimize the switched capacitance at the system level? (8M)
b) How the low power design can be achieved through Voltage Scaling? (6M)

SECTION-III

Q. No. 5 a) Draw the architecture of Carry look ahead Adder and explain its working (6M)
b) Compare Carry Select and Ripple Carry Adders in terms of delay and area (8M)

OR

Q. No.6 Can you construct and explain the low-voltage low-power Logic Styles (14M)

SECTION-IV

Q. No. 7 Elaborate the operation of Baugh-Wooley multiplier with suitable neat sketches (14M)

OR

Q. No. 8 a) Discuss the modified Booth Recoding technique. (8M)
b) What are the building blocks would you choose for binary array multiplier and explain (6M)

SECTION-V

Q. No. 9 a) Briefly explain about techniques at architecture level used to design low power memories (6M)
b) What way would you design the chip architecture of a 1024-bit ROM and explain its operation (8M)

OR

Q. No. 10 a) Discuss the importance of Self-Refresh circuit and explain any one method. (8M)
b) Explain the read and write operations 1-T DRAM cell (6M)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR(S)	PUBLISHERS	EDITION
1	Digital Signal Processing	I,II	Avtar Singh and S. Srinivasan	Thomson Publications	TMH
2	A Practical Approach To Digital Signal Processing	II,III	.Padmanabhan, R.Vijayarajeswan, Ananthi. S	New Age International,	2006/2009
3	Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices	IV	Amy Mar	PHI	2011
4	Embedded Signal Processing with the Micro Signal Architecture Publisher:	V	Woon-Seng Gan, Sen M. Kuo,	Wiley-IEEE Press	2007

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6814

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Regular Examinations, Aug 2017
Digital Signal Processors Architectures
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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Section – I

1. With a neat block diagram, explain the various processes involved in a DSP system. (15m)

OR

2. Compare the terms Dynamic range and Precision. Also, discuss in detail about various A/D conversion errors. (15m)

Section – II

3. Discuss in detail about various DSP Computational building blocks in terms of their functionality and significance. (15m)

OR

4. List out the Salient features of Programmable DSP devices and also explain about the features of external interfacing. (15m)

Section – III

5. Enumerate the concepts related to the Interrupts of TMS320C54XX Processors. (15m)

OR

6. Explain the pipe line operation of TMS320C54XX Processors (15m)

Section –IV

7. List out the important features and applications of Blackfin processor. Also, explain about its Address arithmetic unit. (15m)

OR

8. Discuss in detail about ALM and MAC block diagram and also about Register files of Blackfin Processor. (15m)

Section – V

9. Discuss in detail about Interrupts and I/O with respect to Programmable DSP devices (15m)

OR

10. Explain in detail about Parallel I/o interface and Memory interface with respect to Programmable DSP devices. (15m)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6814 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester supplementary Examinations, Jan/Feb 2018
Digital Signal Processors Architectures
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

Section – I

1. Explain in detail about the Linear time invariant system. Also, give the significance of Compensating filter. (15M)

OR

2. Discuss in detail about the Discrete Fourier transform and fast Fourier Transform with examples. Also, explain the need and advantages of digital filters. (15M)

Section – II

3. Explain the various data addressing capabilities and also, discuss about the speed issues related programmable DSP devices. (15M)

OR

4. Discuss in detail about the Address generating unit. Also, explain about the Programmability of DSP device. (15M)

Section – III

5. Discuss in detail about the Data addressing modes of TMS 320C54xx. Also, explain about on chip Peripherals. (15M)

OR

6. Enumerate the concept involved in memory space of TMS320C54xx Processors.(15M)

Section - IV

7. Discuss in detail about the Architecture of ADSP 2181 high performance Processor(15M)

OR

8. Explain in detail about Blackfin Processor's Bus Architecture and Memory (15M)

Section –V

9. With a neat block diagram, explain about the DMA. (15M)

OR

10. Enumerate the concepts involved in Memory Space Organization.(15M)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6814

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Supplementary Examinations, July/Aug 2018
Digital Signal Processors Architectures
(VLSI&ES)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

SECTION - I

1.	a)	Discuss in detail about number formats for signals and coefficients in DSP systems and explain the difference between them	8M
	b)	What is a system function? Explain how a LTI system is characterized.	7M
		OR	
2.	a)	Explain the phenomenon of sampling rate conversion by a rational factor I/D. Illustrate with necessary diagrams.	8M
	b)	Mention various sources of computational errors and for each category suggest the ways to minimize them in the implementation of DSP systems.	7M
		SECTION – II	
3.	a)	Describe the DSP computational building blocks	8M
	b)	Explain the different features for external interfacing of DSP processors	7M
		OR	
4.	a)	Explain special addressing modes that are provided in DSP processors for real time signal processing with suitable examples.	8M
	b)	Descirbe the Bus Architecture and Memory of Programmable DSP devices	7M
		SECTION – III	
5.	a)	With a neat block diagram, explain in detail about the memory space organization of TMS320C54xx Device	8M
	b)	Discuss in detail about memory and I/O signals of TMS320C54xx Device	7M
		OR	
6.	a)	Explain the interrupts and pipeline operation of TMS320C54XX processors	8M
	b)	Describe the data addressing modes of TMS320C54XX DSPs	7M
		SECTION – IV	
7.	a)	Describe the micro signal architecture of ADSP2181 processor with neat block diagram	8M
	b)	Write short notes on the architecture of Blackfin Processors	7M
		OR	
8.	a)	Describe the Bus architecture and Memory structure of Blackfin processor	8M
	b)	With the help of a neat block diagram, describe the ALU and MAC systems in Analog systems family of DSP devices	7M
		SECTION – V	
9.	a)	Explain about memory space organization.	8M
	b)	Explain about external bus interfacing signals.	7M
		OR	
10.	a)	Explain how DMA method of data transfer help in increasing the processing speed of a DSP processor?	8M
	b)	Explain about interrupts and I/O devices	7M

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

SYSTEM ON CHIP ARCHITECTURE
COURSE COVERAGE SUMMARY

S.NO	TEXT BOOK TITLE	Units / Topics Covered	AUTHOR	PUBLISHERS	EDITION
1	Computer System Design System-on-Chip	I,II,III,IV,V	J. Flynn and Wayne Luk	Wiely India Pvt. Ltd.	
2	ARM System on Chip Architecture	IV	Steve Furber	Addison Wesley Professional.	2 nd Ed., 2000,
3	Design of System on a Chip: Devices and Components –	III,V	Ricardo Reis	Springer	1 st Ed., 2004,

DESIGN FOR TESTABILITY

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR(S)	PUBLISHERS
1	Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits	I,II	M.L. Bushnell, V. D. Agrawal	KluwerAcademic Pulishers.
2	Digital Systems and Testable Design -	III,IV,V	M.Abramovici,M.A.Breuer and A.D Frieman	Jaico Publishing House
3	Digital Circuits Testing and Testability - P.K. Lala, Academic Press..	I,II	P.K. Lala,	Academic Press

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6817

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Regular Examinations, Aug 2017
Design For Testability
(Common to VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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Section – I

1. Discuss in detail about the VLSI Technology trends affecting testing. (15m)

OR

2. Bring out the difference between Functional and Structural testing. (15m)

Section - II

3. List out and explain about the various steps involved in Test Evaluation. (15m)

OR

4. What are the various algorithms for Fault simulation and explain any two of them in detail. (15m)

Section – III

5. Discuss in detail about SCOAP Controllability and Observability and give their significance to testability measures. (15m)

OR

6. Explain in detail about Partial – Scan design and Scan design. (15m)

Section – IV

7. Explain and give the significance of memory BIST. (15m)

OR

8. Discuss about the Test per clock and Test – per Scan BIST systems. (15m)

Section - V

9. Discuss in detail about Boundary Scan description language. (15m)

OR

10. Explain in detail about the Pin constraints of the standout and pin descriptions. (15m)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6817 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester supplementary Examinations, Jan/Feb 2018
Design for Testability
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

****

Section – I

1. Discuss about the Single stuck at Fault with example and also explain about various levels of Fault models. (15m)

OR

2. Explain in detail about the various types of testing and the role of testing. (15m)

Section - II

3. List out and explain about the various steps involved in Simulation for design verification . (15m)

OR

4. What are the various algorithms for true – value simulation and explain any one of them in detail. (15m)

Section - III

5. What are the various High level testability measures and explain about them. (15m)

OR

6. Discuss in detail about Ad – Hoc DFT methods . (15m)

Section – IV

7. Enumerate the concept involved in the Built – In logic block observers and BIST Process.(15m)

OR

8. Discuss in detail about circular self test path system with an example. (15m)

Section - V

9. Discuss in detail about the TAP Controller and Port in terms of its significance, principle involved, advantages and limitations. (15m)

OR

10. Explain in detail about the Boundary Scan Test instructions. (15m)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D6817 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Supplementary Examinations, July/Aug 2018
Design for Testability
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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SECTION – I

1. Explain in detail about Digital and Analog VLSI Testing and give the VLSI technology trends affecting testings . (15M)

OR

2. Compare the Functional and Structural testing. Also, discuss about various types of testing, (15M)

SECTION - II

3. Discuss the problems in Simulation Based Design verification. (15M)

OR

4. List out the various General Fault Simulation techniques and explain in detail about any one of them. (15M)

SECTION - III

5. Discuss the concepts related to Partial Scan Design and Variations of Scan. (15M)

OR

6. Explain in detail about High level Testability measures and Observability. (15M)

SECTION - IV

7. Give a logic design for the BIST hardware required to support the STUMPS methodology at the board level. Assume each chip is designed with a single scan path. Thus every LFSR must be placed into one or more 'STUMPS' chips. (15M)

OR

8. Explain in detail about Memory BIST and delay Fault BIST. (15M)

SECTION - V

9. Explain in detail about TAP controller and Boundary Scan instructions. (15M)

OR

10. Discuss in detail about BDSL description components and Pin Descriptions (15M)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D6817 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Regular Examinations, July/Aug 2018
Design for Testability
(VLSI &ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

*****

SECTION-I

Q. No. 1 a) Explain the role of testing in VLSI realization process. (6M)
b) How could you reduce the single stuck at faults? Can you elaborate the concepts with examples (8M)

OR

Q. No. 2 a) Define testing? Outline the types of Testing? (5M)
b) Can you distinguish between Defects, Errors, and Faults with relevant examples? (9M)

SECTION-II

Q. No. 3 a) Can you explain the purpose of Simulation for Design Verification with block diagram (6M)
b) Discuss the timing modeling of circuits with an example (8M)

OR

Q. No. 4 a) Why the compiled-code simulators is usually limited to high-level design verification? (4M)
b) Can you elaborate on the reason why the Event-driven simulation is a very effective procedure for discrete-event simulation with detailed example? (10M)

SECTION-III

Q. No. 5 Can you explain elaborately how the combinational SCOAP controllability and observability was calculated for all gates with an example? (14M)

OR

Q. No.6 a) Discuss about AdHoc design for testability methods? (4M)

b) Can you elaborate the main idea of scan design and illustrate the scan design and test generation with an example? (10M)

SECTION-IV

Q. No. 7 a) Distinguish and discuss about Test-Per-Scan BIST Systems (8M)
b) Explain the delay fault BIST testing system (6M)

OR

Q. No. 8 Categorize the Memory BIST techniques and Discuss elaborately. (14M)

SECTION-V

Q. No. 9 a) Explain the Board-Level Bus Testing (6M)
b) Explain the advantages of BSDL and describe the BSDL entity (8M)

OR

Q. No. 10 a) Explain the purpose of Boundary scan Standard. (4M)
b) Discuss the Pin Constraints of the boundary scan /JTAG Standard (10M)

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

ADHOC WIRELESS NETWORKS

COURSE COVERAGE SUMMARY

S.NO	TEXT BOOK TITLE	UNITS /TOPICS COVERED	AUTHOR(S)	PUBLISHERS
1	Ad Hoc Wireless Networks: Architectures and Protocols	I-IV	C. Siva Ram Murthy and B.S.Manoj	2004, PHI
2	Wireless Ad-hoc and Sensor Networks: Protocols, Performance and Control	V	Jagannathan Sarangapani	CRC Press.

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D9310 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester supplementary Examinations, Jan/Feb 2018
Adhoc- Wireless Networks
(SSP)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

Section-I

1 a) Explain about various functionalities of the MAC layer used in IEEE 802.11 WLANs. 10 M
b) What are the services offered by a typical IEEE 802.11 Network? Explain in detail. 5 M

OR

2 a) Explain the operation of EY-NPMA with a neat diagram. 10 M
b) What are the various applications of Ad hoc wireless networks? 5 M

Section-II

3 a) What are the main issues that need to be addressed while designing a MAC protocol for Ad hoc wireless networks? 10 M
b) Explain the operation of DMAC protocol with neat diagrams. 5 M

OR

4 a) Explain about any two Contention-based MAC protocols with reservation mechanisms. 10 M
b) What are the important design goals of a MAC protocol for Ad hoc wireless networks? 5 M

Section-III

5 a) Explain about any two Table Driven Routing protocols. 10 M
b) What are the characteristics of an Ideal Routing Protocol for Ad Hoc Wireless Networks? 5 M

OR

6 Explain in detail about PLBR and HSR protocols. 15 M

Section-IV

7 a) Explain about various issues and design goals of TCP for Ad hoc wireless networks. 10 M
b) Explain about Ad hoc transport protocol in detail. 5 M

OR

8 a) What are the techniques to be used to improve the performance of TCP in Ad hoc wireless networks? Explain in detail. 15 M

Section-V

9 a) What do you mean by data gathering? Explain the algorithms that implement data gathering. 10 M
b) What are the three basic MAC protocols used in sensor networks? Explain. 5 M

OR

10 a) Explain about Indoor Localization and Sensor Network Localization. 10 M
b) Compare Sensor networks and Ad hoc wireless networks. 5 M

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R15D9310 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018
Adhoc- Wireless Networks
(CSE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

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Section-I

1. a) Describe the services provided by Bluetooth
   b) Explain the Analog modulation techniques. (8+7M)

OR

2. a) Explain HIPERLAN MAC Sub layer
   b) What are the various issues and challenges that are to be considered to design a ad-hoc wireless system? (7+8M)

Section-II

3. a) Explain the role of directional antennas in MAC protocols
   b) What are main issues that are to be considered to design a MAC protocol for adhoc wireless networks?(7+8M)

OR

4. a) Explain contention based scheduling mechanisms
   b) How does the packet queueing mechanism of MACA differ from that of MACAW? Which one of them is better? Why? (7+8M)

Section-III

5. a) Describe about various types of hybrid routing protocols
   b) Explain DSR protocol with an example.(7+8M)

OR

6. a) List out various issues in designing a routing protocol for Ad hoc wireless networks
   b) Explain AODV protocol with an example.(7+8M)

Section-IV

7. a) Discuss the various TCP solutions for ad-hoc wireless networks
   b) Discuss the design goals of transport layer protocols for adhoc wireless networks .(8+7M)

OR

8. a) write the comparison of TCP solutions for Adhoc wireless networks
   b) Explain Adhoc TCP and also specify its advantages and disadvantages. (7+8M)

Section-V

9. a) Explain location discovery in wireless sensor networks
   b) Write the issues and challenges in designing wireless sensor networks. (8+7M)

OR

10. a) Explain the sensor network layered architecture
    b) Explain the quality of a sensor network. (8+7M)

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Code No: R15D9310

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester supplementary Examinations, July/Aug2018
Adhoc- Wireless Networks
(SSP)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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SECTION-I

Q. No. 1 a) List the various topologies used in physical design and explain. 8M
b) Discuss various 802.11 standards defined for wireless network. 7M

OR

Q. No. 2 a) Explain the Wireless PAN working group. 7M
b) Explain the Bluetooth technology and connection establishment in Bluetooth 8M

SECTION-II

Q. No. 3 Explain the major issues to be considered in designing a MAC protocol for Ad hoc wireless networks. 15M

OR

Q. No. 4 a) Explain MAC protocol using directional antennas? 5M
b) Explain in detail about Contention based protocols with scheduling mechanism. 10M

SECTION-III

Q. No. 5 a) Give the classification of routing protocols. 5M
b) Explain the Routing Protocols with Efficient Flooding Mechanisms 10M

OR

Q. No. 6 Explain the various Table –Driven Routing Protocols. 15M

SECTION-IV

Q.No.7a)Discuss various Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks. 8M
b)What are the Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, explain in detail 7M

OR

Q. No. 8 Write short notes on
a) Application Controlled Transport Protocol 8M
b) Ad Hoc Transport Protocol 7M

SECTION-V

Q. No. 9 a) with an example, explain the Rumor Routing algorithm. 7M
b) Describe two basic mechanisms of location discovery. 8M

OR

Q. No. 10 Briefly describe various data gathering algorithms. 15M

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17D9310

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Regular Examinations, July/Aug 2018
Adhoc-Wireless Networks
(VLSI &ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

Q. No. 1 a) Write about the design goals of WLANs? [7M]
b) Explain Bluetooth in detail. [7M]

OR

Q. No. 2 a) Explain fundamentals of WLANs'? [7M]
b) Explain the functionalities that the MAC layer provides in IEEE 802.11 WLANs? [7M]

SECTION-II

Q. No. 3 a) While designing a MAC protocol for adhoc wireless networks, explain the issues that needs to addressed? [7M]
b) What are the important goals to be met while designing a MAC protocol for adhoc wireless networks? [7M]

OR

Q. No. 4 a) Draw the frame structure in five phase reservation protocol and explain the phases of the reservation process? [7M]
b) With a diagram, explain the data transmission mechanism in multiple access collision technique? [7M]

SECTION-III

Q. No. 5 a) Broadly classify routing protocols for adhoc wireless networks and briefly explain? [7M]
b) Explain any one hybrid routing protocols with an example [7M]

OR

Q. No. 6 a) With an example, explain the destination sequenced distance vector routing protocol? [7M]
b) With an example, explain the optimized link state routing protocol? [7M]

SECTION-IV

Q. No. 7 a) Name the important goals to be met while designing a transport layer protocol for wireless networks? [7M]
b) Classify and briefly explain transport layer protocol? [7M]

OR

Q. No. 8 a) Explain the issues to be considered while designing transport layer protocol for adhoc wireless networks? [7M]

b) Name the reasons behind through put degradation that TCP faces when used in adhoc wireless networks? [7M]

SECTION-V

Q. No. 9 a) Classify and draw the tree structure of sensor network protocols? [7M]

b) Explain the issues and challenges in designing a sensor network? [7M]

OR

Q. No. 10 a) Explain data dissemination ? [7M]

b) Explain data gathering? [7M]

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – (VLSI & Embedded Systems)

Code No: R17DEC52

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Regular Examinations, July/Aug 2018
Internet of Things
(VLSI &ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION – I

1. Discuss in detail about IP addressing and subnetting. (14M)

OR

2. Explain in detail about Point to Point Data transfer and Point to Multi Point Data transfer. (14M)

SECTION - II

3. Enumerate in detail the concepts related to Networking configurations in Linux accessing Hardware and Device files interactions. (14M)

OR

4. Discuss in detail about the Wired Networking equipments. (14M)

SECTION - III

5. Discuss in detail about the 6Lo W PAN. (14M)

OR

6. List out the Salient features of IOT Architecture and explain about Web of Things. (14M)

SECTION - IV

7. Discuss in detail about application protocols related to MQTT, CoAP (14M)

OR

8. Discuss in detail about REST and HTTP (14M)

SECTION - V

9. Discuss in detail about Use of Big Data and Visualization in IOT. (14M)

OR

10. Explain in detail about Sensors and Sensor Mode and interfacing using Raspberry Pi. (14M)

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